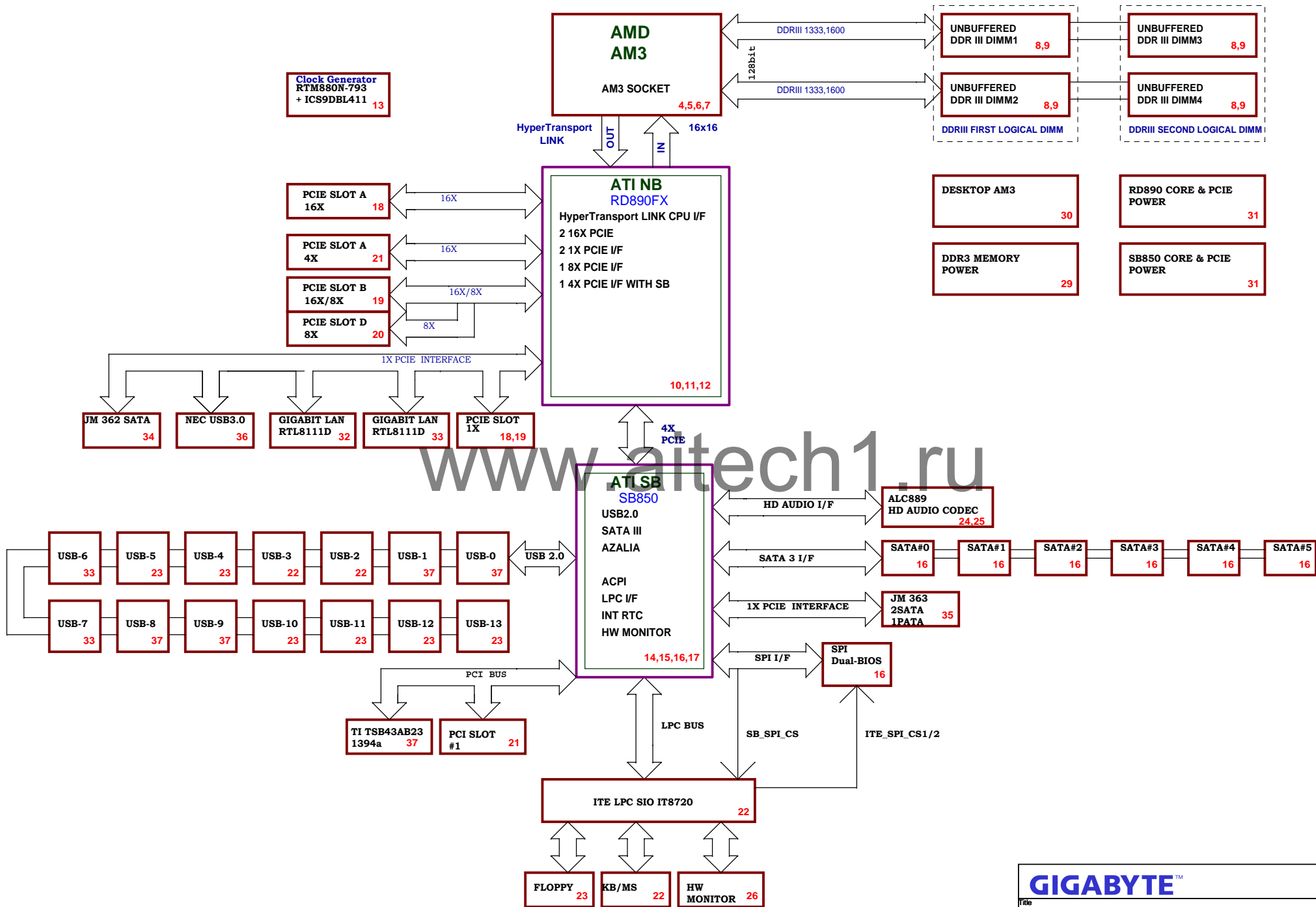
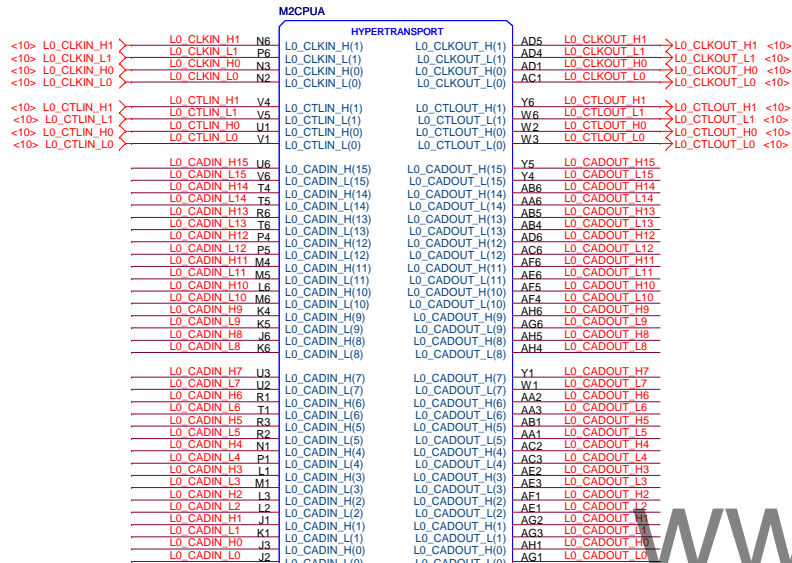


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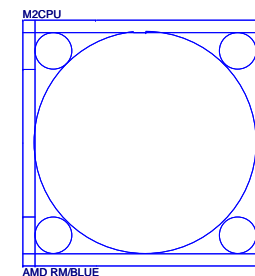
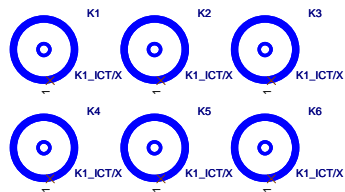
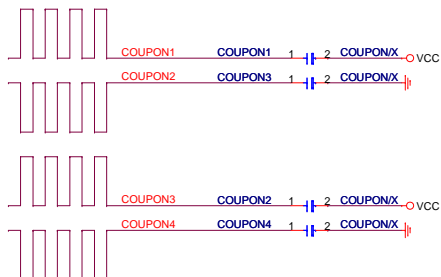
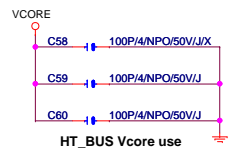
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L0_CADIN_L[0..15] <L0_CADIN_L[0..15] <10>
 L0_CADIN_H[0..15] <L0_CADIN_H[0..15] <10>
 L0_CADOUT_L[0..15] <L0_CADOUT_L[0..15] <10>
 L0_CADOUT_H[0..15] <L0_CADOUT_H[0..15] <10>



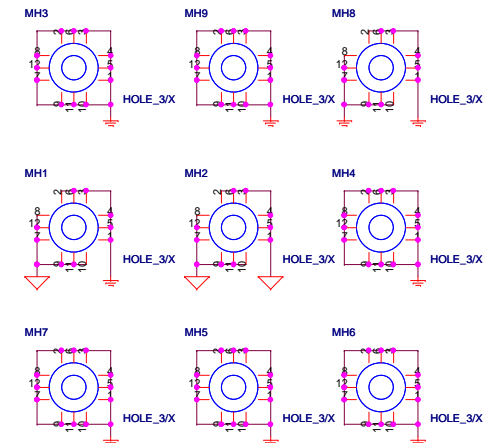
CPU-SK941AM3S/GF[10SC1-A01941-04R_10SC1-A01941-05R]



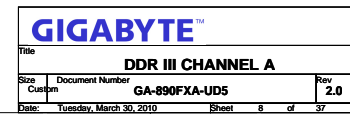
CPU_VDD_RUN = VCORE
 CPU_VDDA_RUN = VDDA25
 VLDT_RUN = VCC12_HT
 CPU_VDDIO_SUS = DDR15V
 CPU_VDDR = CPU_VDDR12

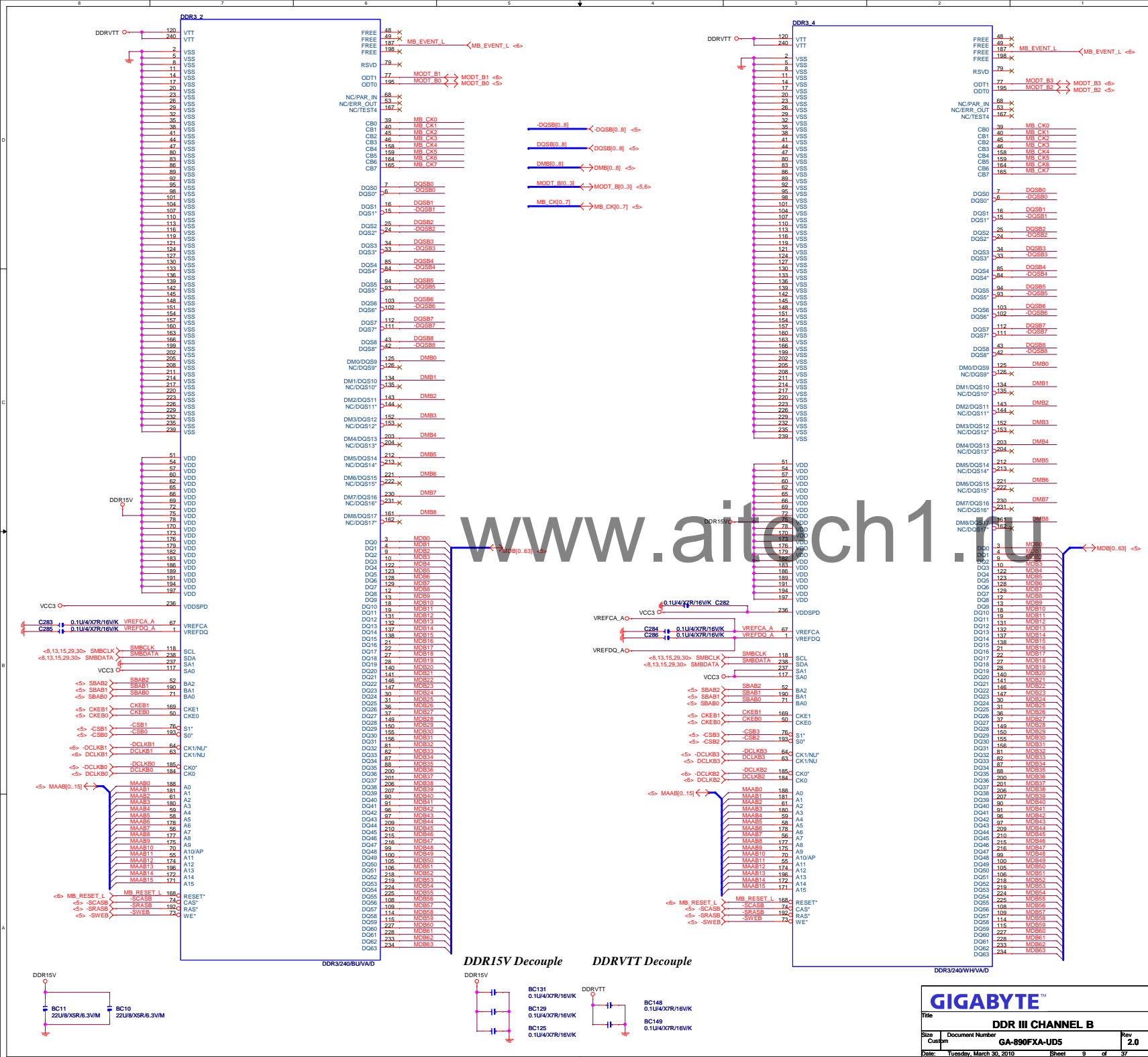
VLDT_A = VCC12_HT
 VLDT_B = HT12B

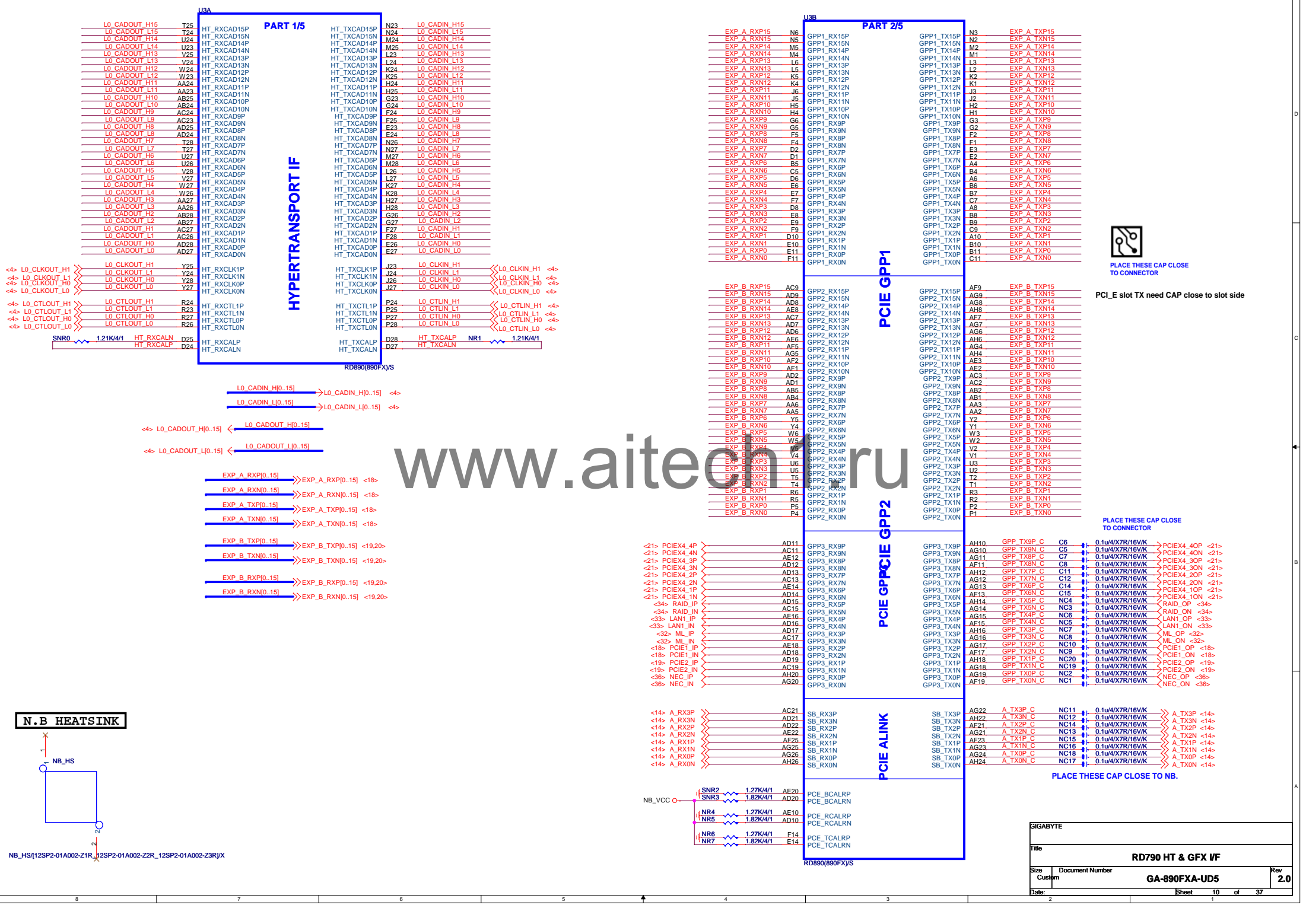
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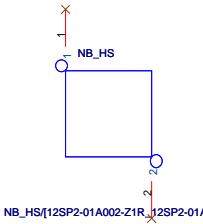
GIGABYTE™			
Title CPU HYPER TRANSPORT			
Size Custom	Document Number GA-890FXA-UD5	Rev 2.0	
Date: Tuesday, March 30, 2010	Sheet 4	of 37	







N.B HEATSINK



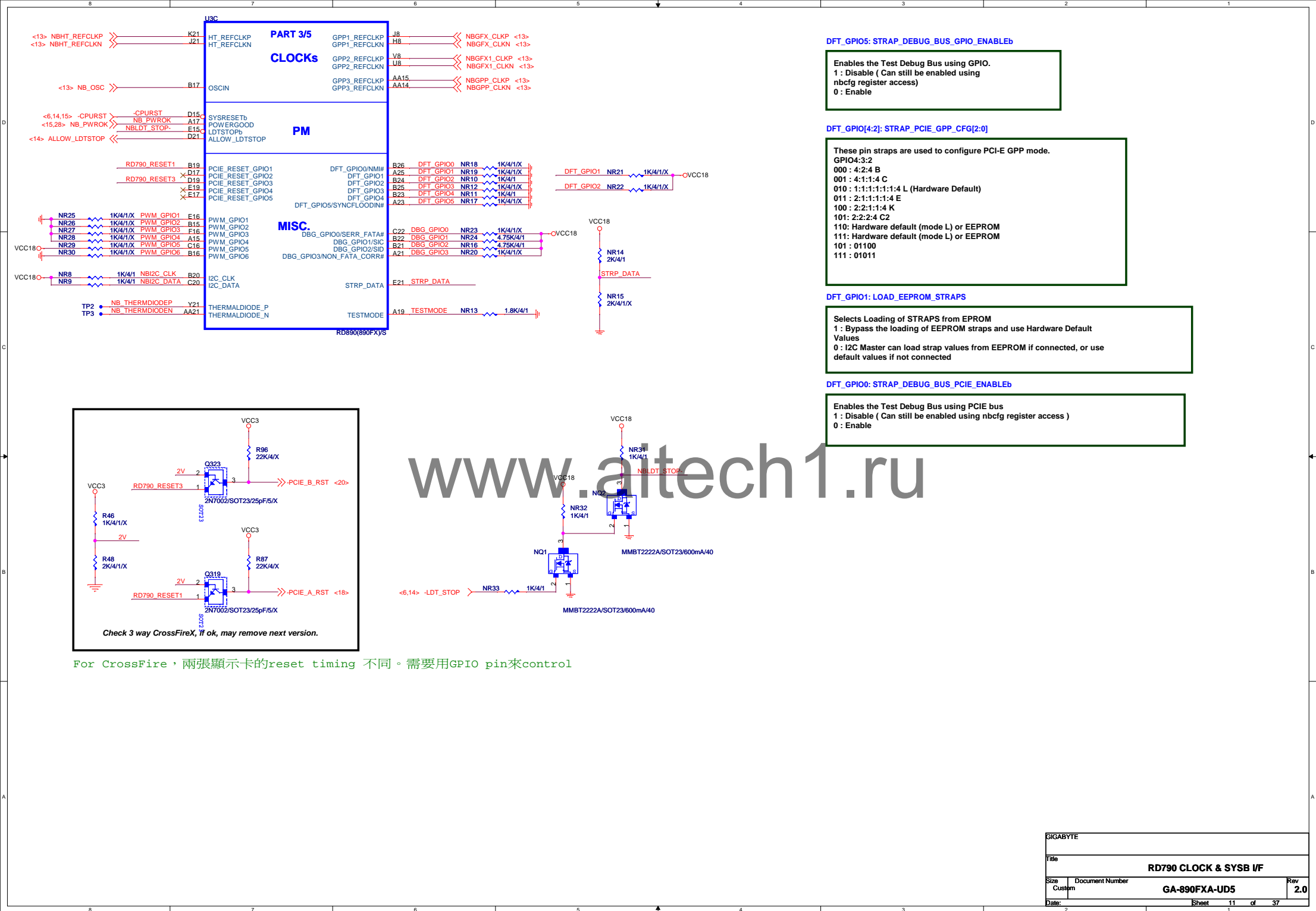
PLACE THESE CAP CLOSE TO CONNECTOR

PCI E slot TX need CAP close to slot side

PLACE THESE CAP CLOSE TO CONNECTOR

PLACE THESE CAP CLOSE TO NB.

GIGABYTE			
Title			
RD790 HT & GFX IF			
Size	Document Number	Rev	
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Date:	Sheet	10	of 37



PART 3/5
CLOCKS

PM

MISC.

DFT_GPIO5: STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

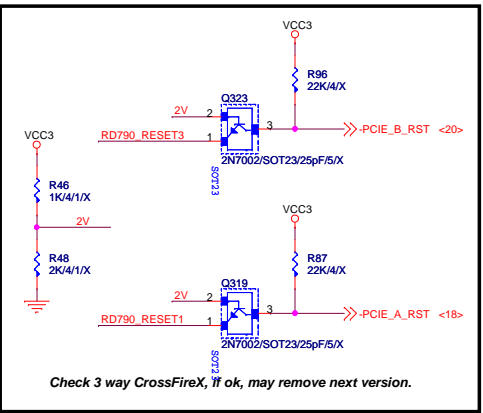
These pin straps are used to configure PCI-E GPP mode.
GPIO4:3:2
000 : 4:2:4 B
001 : 4:1:1:4 C
010 : 1:1:1:1:1:4 L (Hardware Default)
011 : 2:1:1:1:1:4 E
100 : 2:2:1:1:4 K
101 : 2:2:2:4 C2
110: Hardware default (mode L) or EEPROM
111: Hardware default (mode L) or EEPROM
101 : 01100
111 : 01011

DFT_GPIO1: LOAD_EEPROM_STRAPS

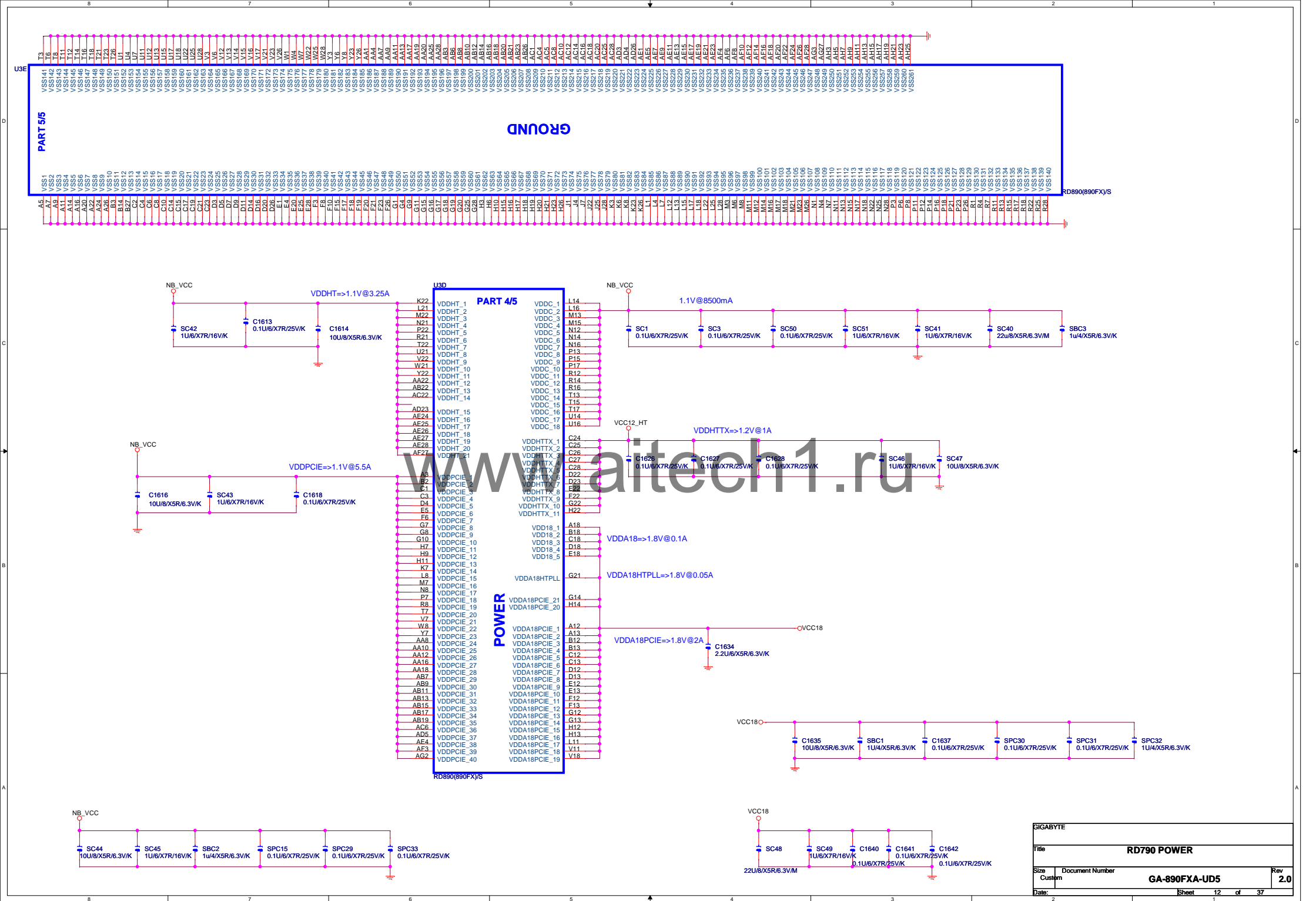
Selects Loading of STRAPS from EPROM
1 : Bypass the loading of EEPROM straps and use Hardware Default Values
0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

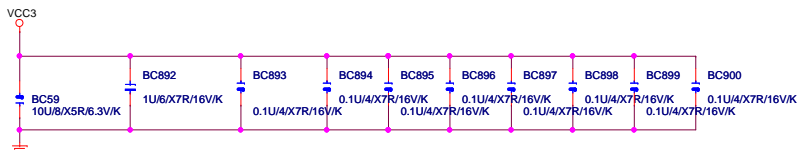
DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

Enables the Test Debug Bus using PCIE bus
1 : Disable (Can still be enabled using nbcfg register access)
0 : Enable



For CrossFire, 兩張顯示卡的reset timing 不同。需要用GPIO pin來control

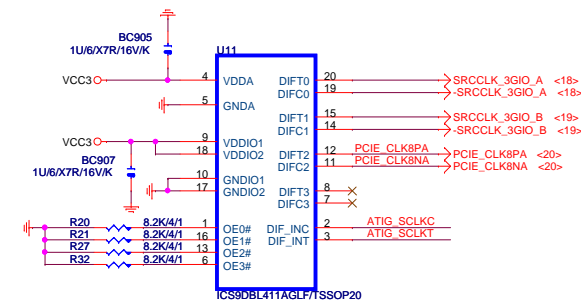
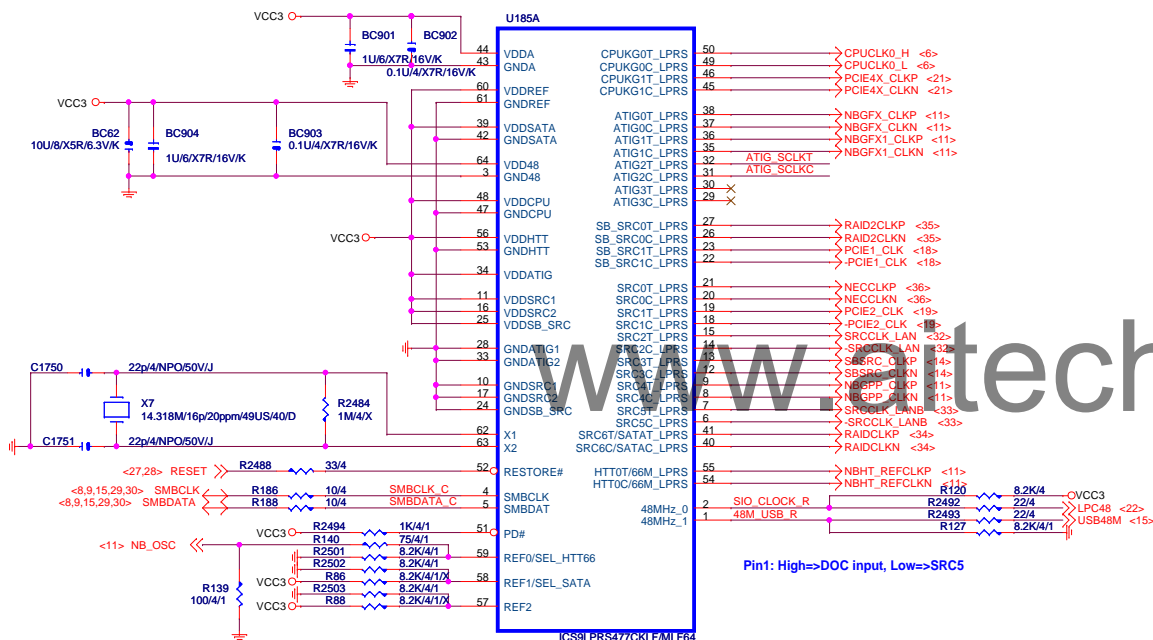




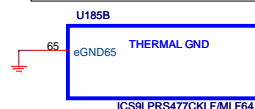
NB CLOCK INPUT TABLE

NB CLOCKS	RS740	RX780	RS780
HT_REFCLKP	66M SE(SE)	100M DIFF	100M DIFF
HT_REFCLKN	NC	100M DIFF	100M DIFF
REFCLK_P	14M SE (3.3V)	14M SE (1.8V)	14M SE (1.1V)
REFCLK_N	NC	vref	100M DIFF
GFX_REFCLK*	100M DIFF	100M DIFF	100M DIFF
GPP_REFCLK	NC	100M DIFF	100M DIFF(OUT)
GPSPB_REFCLK	100M DIFF	100M DIFF	100M DIFF

* the GFX_REFCLK input is required for all cases



Clock chip has internal serial terminations for differential pairs, external resistors are reserved for debug purpose.



	OSC_14M_NB
RS740	3.3V 33R serial
RX780	1.8V 82.5R/130R
RS780 (Single-ended)	1.1V 158R/90.9R

REF0/SEL_HTT66	HTT CLOCK
0	100.00 DIFFERENTIAL
1	66.66 SINGLE END

REF1/SEL_SATA	SRC6/SATA
0	100.00 DIFFERENTIAL SPREADING SRC CLOCK
1	100.00 NON-SPREADING DIFFERENTIAL SATA CLOCK

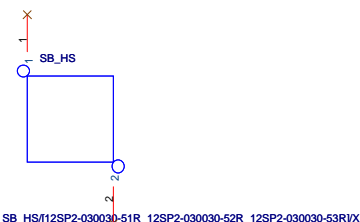
GIGABYTE™

Title: **ICS9LPRS477**

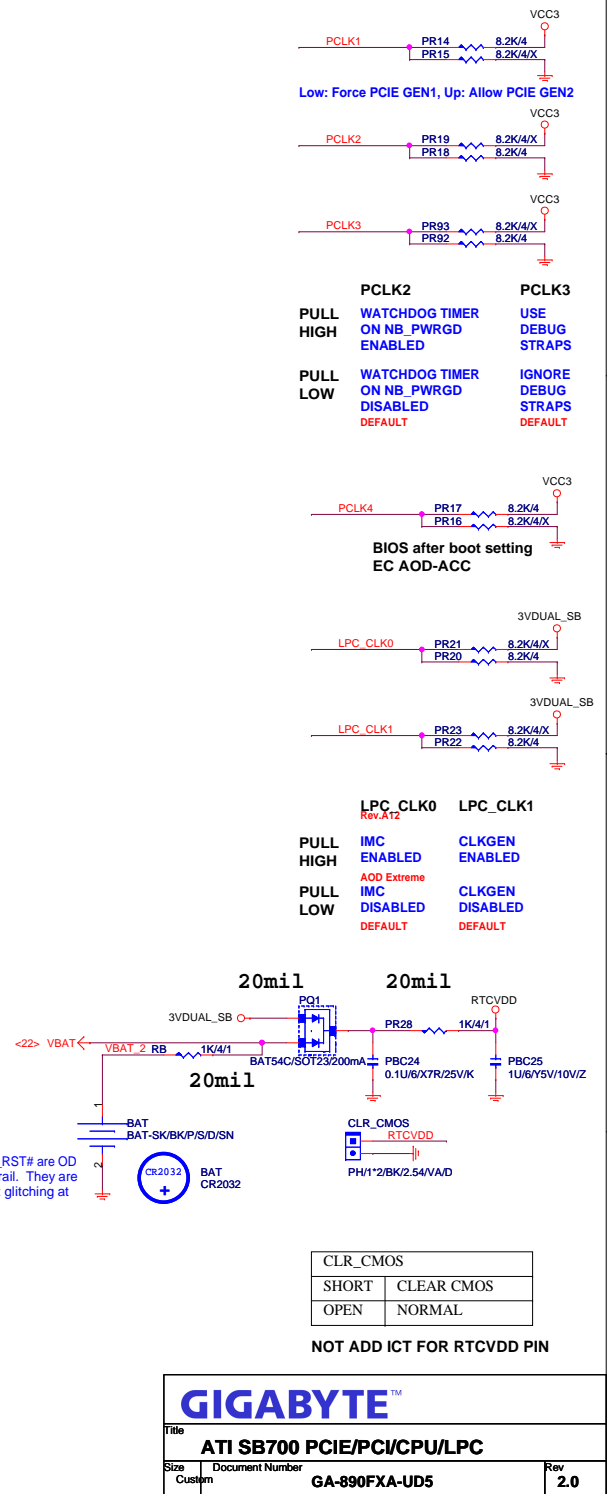
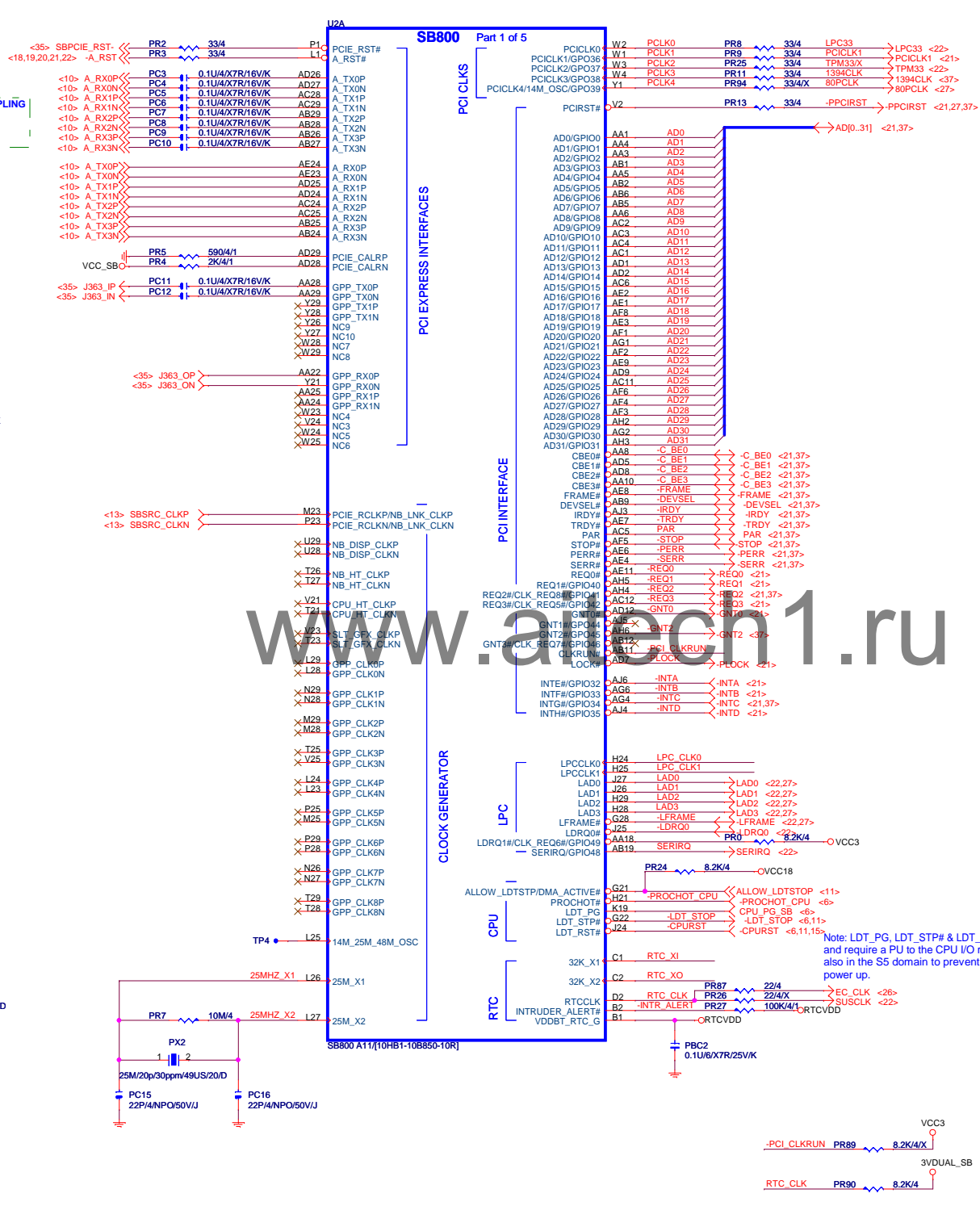
Size: Custom Document Number: **GA-890FXA-UD5** Rev: **2.0**

Date: Tuesday, March 30, 2010 Sheet 13 of 37

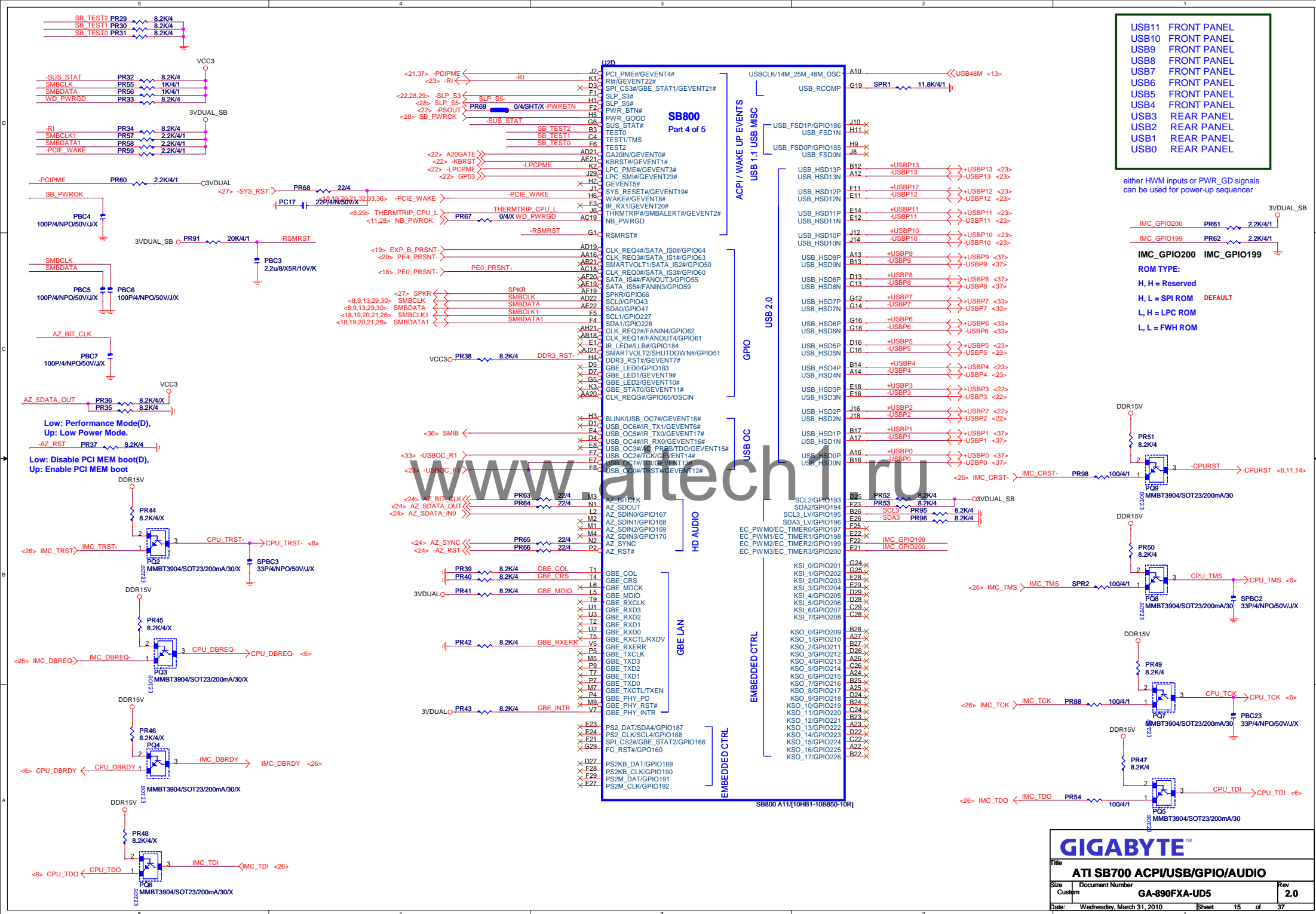
S.B HEATSINK



SHW/D0.64*5.08*6.74



GIGABYTE		
Title ATI SB700 PCIE/PCI/CPU/LPC		
Size Custom	Document Number GA-890FXA-UD5	Rev 2.0
Date: Tuesday, March 30, 2010	Sheet 14	of 37





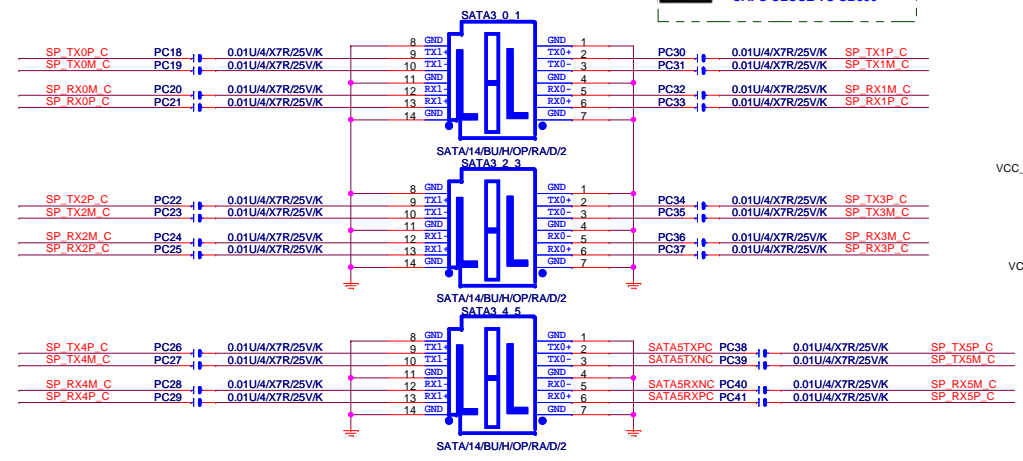
PLACE SATA CAL
RES VERY CLOSE
TO BALL OF U600

NOTE:
R650 IS 1K 1% FOR 25MHz
XTAL, 4.99K 1% FOR 100MHz
INTERNAL CLOCK

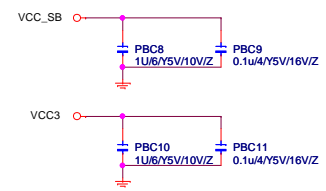


<22> -SB_SPL_CS_ITE <<

SB_SPL_DI PR70 22/4 SB_SPL_DI_R 35
SB_SPL_DO PR71 22/4 SB_SPL_DO_R 35
SB_SPL_CLK PR72 22/4 SB_SPL_CLK_R 35
SB_SPL_CS_ITE PR73 22/4 SB_SPL_CS_ITE 35

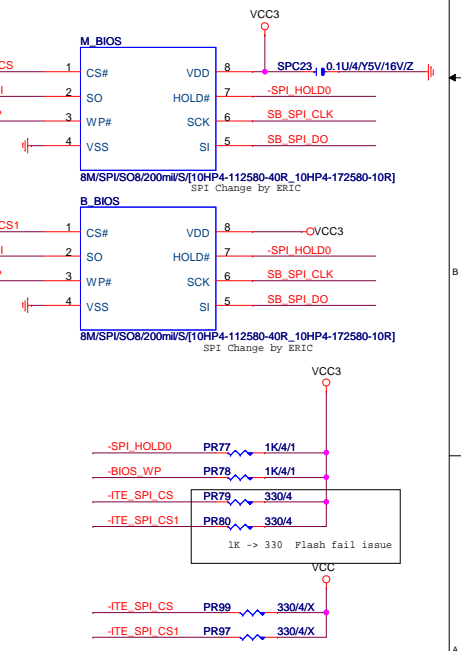


PLACE SATA AC COUPLING
CAPS CLOSE TO SB850

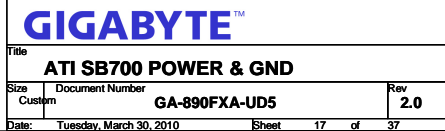


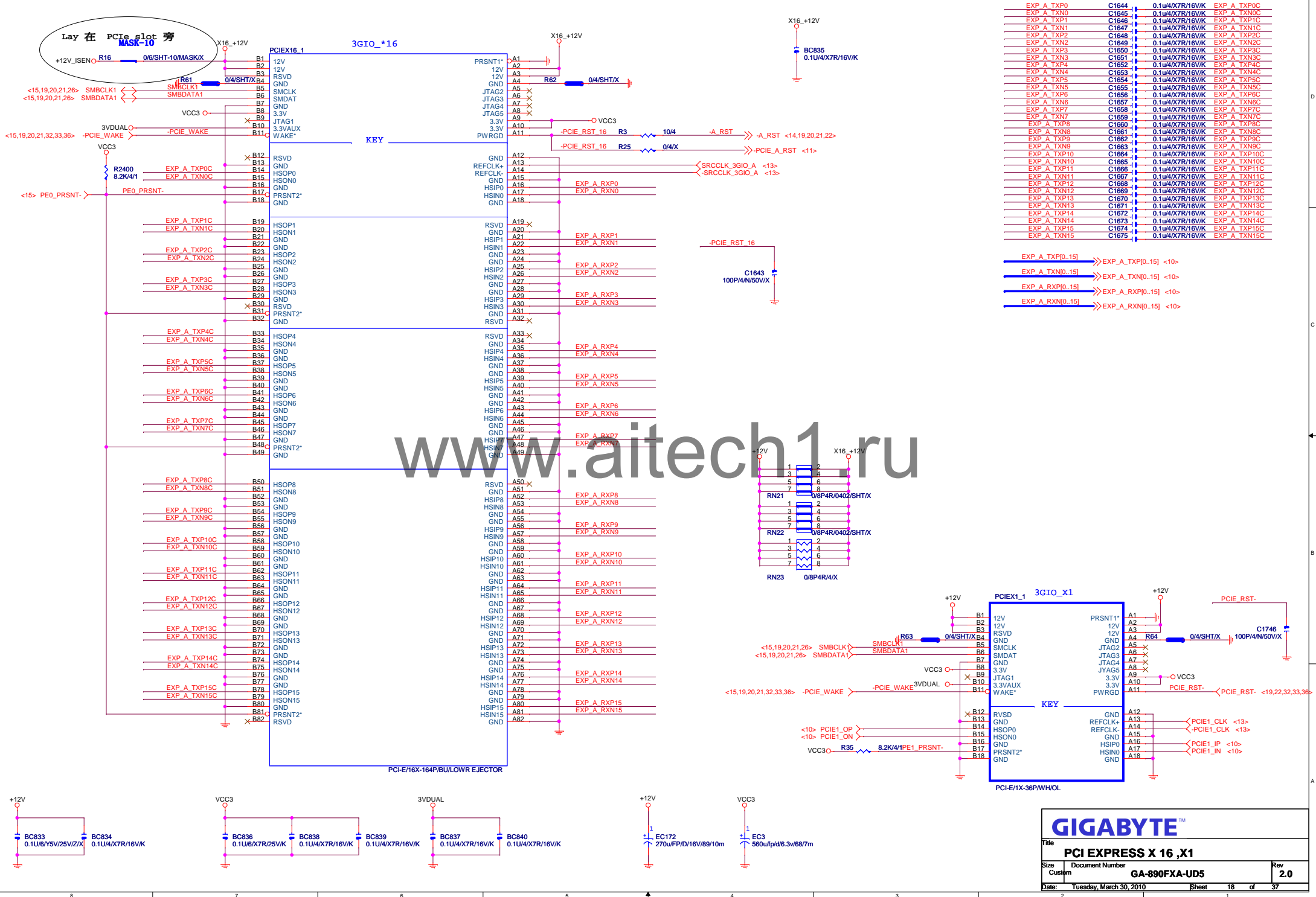
GIGABYTE™

Title ATI SB700 SATA/IDE/HWM/SPI		
Size Custom	Document Number GA-890FXA-UD5	Rev 2.0
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EXP A TXP0	C1644	0.1u4/X7R/16V/K	EXP A TXP0C
EXP A TXN0	C1645	0.1u4/X7R/16V/K	EXP A TXN0C
EXP A TXP1	C1646	0.1u4/X7R/16V/K	EXP A TXP1C
EXP A TXN1	C1647	0.1u4/X7R/16V/K	EXP A TXN1C
EXP A TXP2	C1648	0.1u4/X7R/16V/K	EXP A TXP2C
EXP A TXN2	C1649	0.1u4/X7R/16V/K	EXP A TXN2C
EXP A TXP3	C1650	0.1u4/X7R/16V/K	EXP A TXP3C
EXP A TXN3	C1651	0.1u4/X7R/16V/K	EXP A TXN3C
EXP A TXP4	C1652	0.1u4/X7R/16V/K	EXP A TXP4C
EXP A TXN4	C1653	0.1u4/X7R/16V/K	EXP A TXN4C
EXP A TXP5	C1654	0.1u4/X7R/16V/K	EXP A TXP5C
EXP A TXN5	C1655	0.1u4/X7R/16V/K	EXP A TXN5C
EXP A TXP6	C1656	0.1u4/X7R/16V/K	EXP A TXP6C
EXP A TXN6	C1657	0.1u4/X7R/16V/K	EXP A TXN6C
EXP A TXP7	C1658	0.1u4/X7R/16V/K	EXP A TXP7C
EXP A TXN7	C1659	0.1u4/X7R/16V/K	EXP A TXN7C
EXP A TXP8	C1660	0.1u4/X7R/16V/K	EXP A TXP8C
EXP A TXN8	C1661	0.1u4/X7R/16V/K	EXP A TXN8C
EXP A TXP9	C1662	0.1u4/X7R/16V/K	EXP A TXP9C
EXP A TXN9	C1663	0.1u4/X7R/16V/K	EXP A TXN9C
EXP A TXP10	C1664	0.1u4/X7R/16V/K	EXP A TXP10C
EXP A TXN10	C1665	0.1u4/X7R/16V/K	EXP A TXN10C
EXP A TXP11	C1666	0.1u4/X7R/16V/K	EXP A TXP11C
EXP A TXN11	C1667	0.1u4/X7R/16V/K	EXP A TXN11C
EXP A TXP12	C1668	0.1u4/X7R/16V/K	EXP A TXP12C
EXP A TXN12	C1669	0.1u4/X7R/16V/K	EXP A TXN12C
EXP A TXP13	C1670	0.1u4/X7R/16V/K	EXP A TXP13C
EXP A TXN13	C1671	0.1u4/X7R/16V/K	EXP A TXN13C
EXP A TXP14	C1672	0.1u4/X7R/16V/K	EXP A TXP14C
EXP A TXN14	C1673	0.1u4/X7R/16V/K	EXP A TXN14C
EXP A TXP15	C1674	0.1u4/X7R/16V/K	EXP A TXP15C
EXP A TXN15	C1675	0.1u4/X7R/16V/K	EXP A TXN15C

EXP A TXP0..15]	>>>EXP_A_TXP[0..15]	<10>
EXP A TXN0..15]	>>>EXP_A_TXN[0..15]	<10>
EXP A RXP0..15]	>>>EXP_A_RXP[0..15]	<10>
EXP A RXN0..15]	>>>EXP_A_RXN[0..15]	<10>

GIGABYTE™

Title

PCI EXPRESS X 16, X1

Size

Custom

Document Number

GA-890FXA-UD5

Rev

2.0

Date:

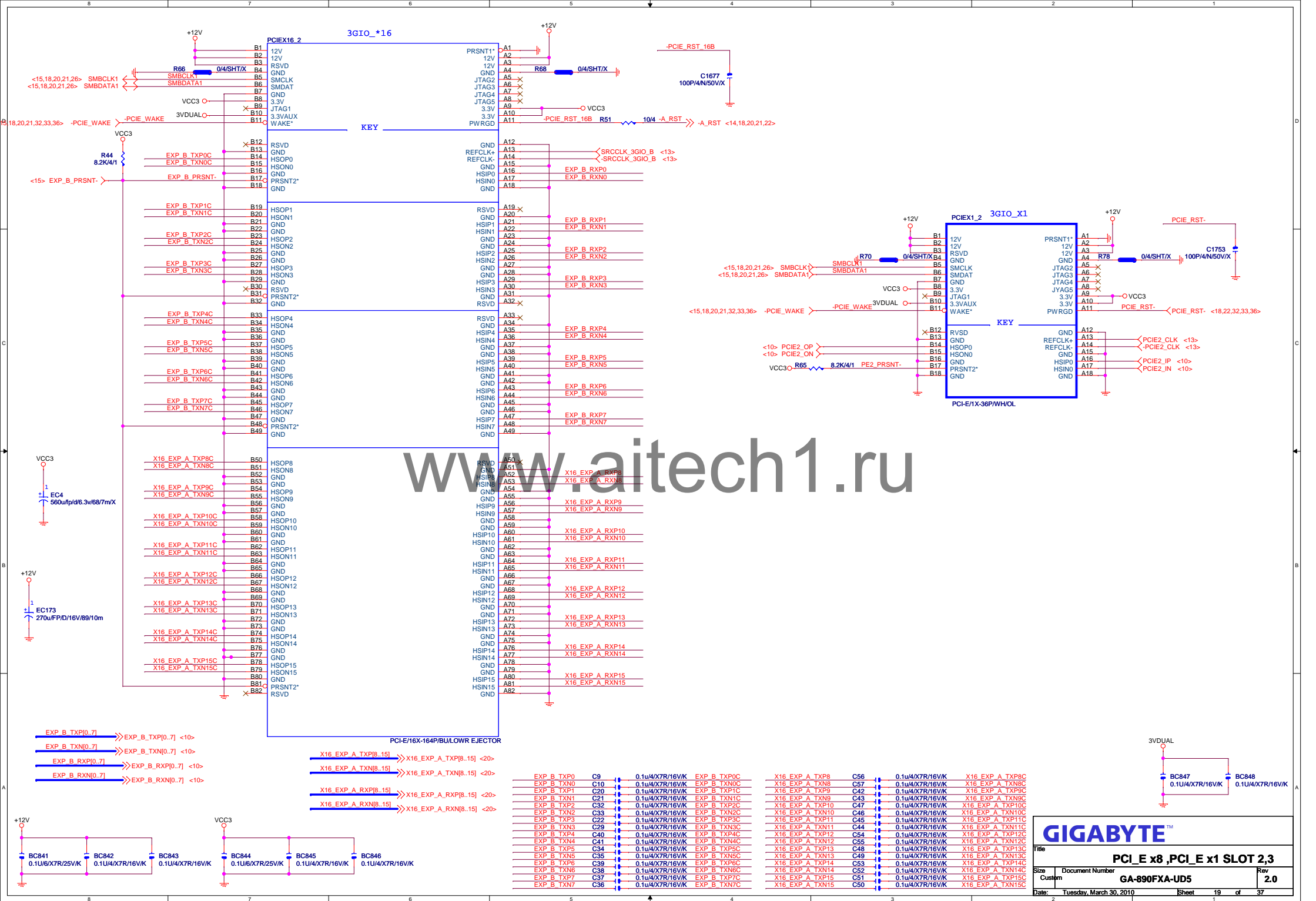
Tuesday, March 30, 2010

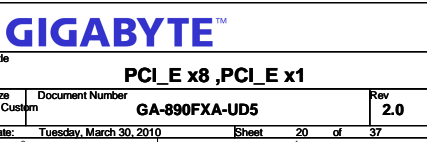
Sheet

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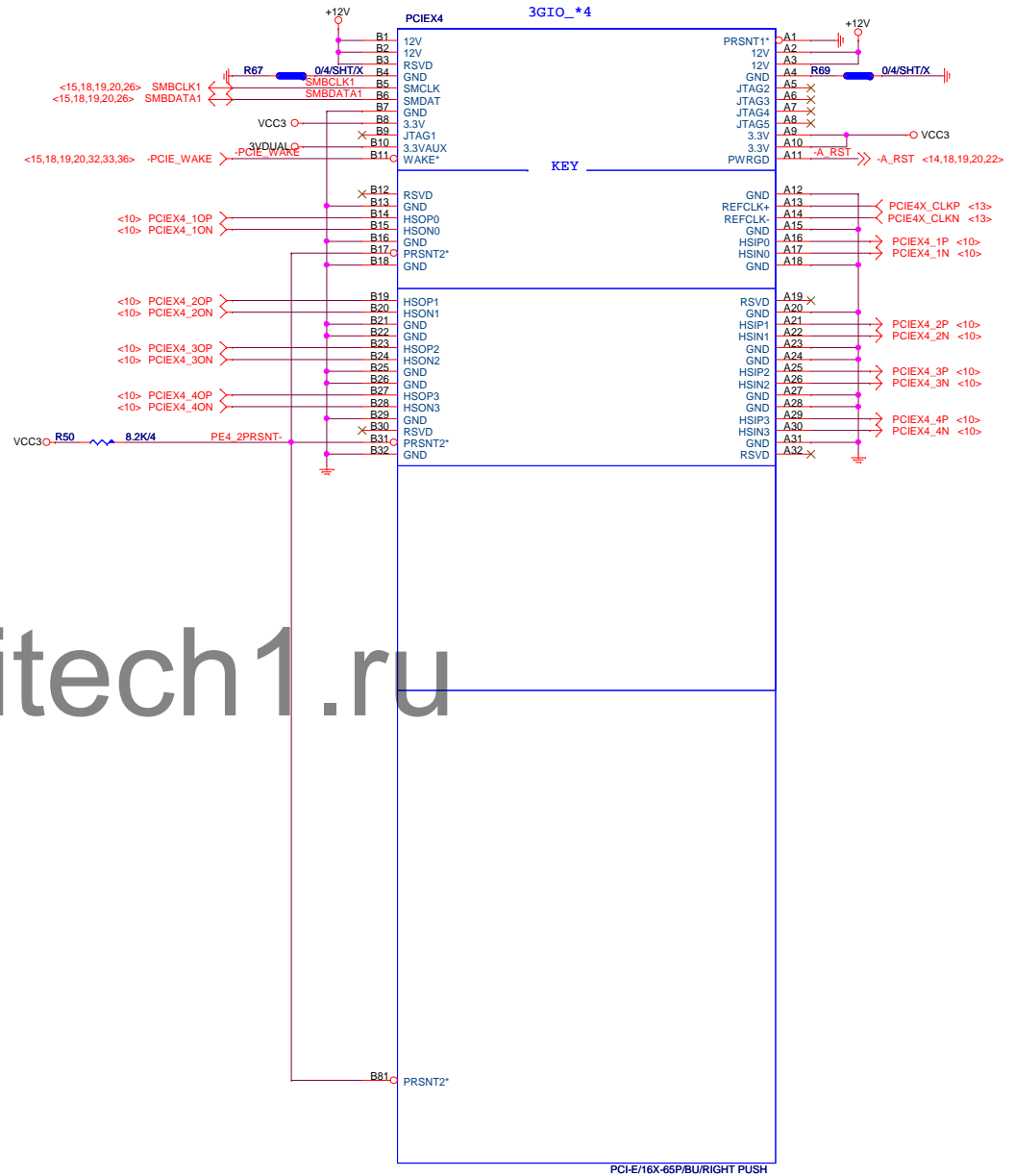
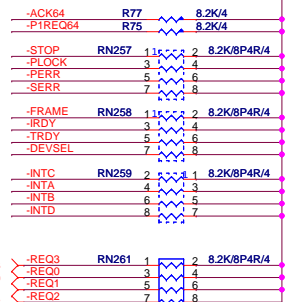
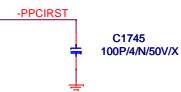
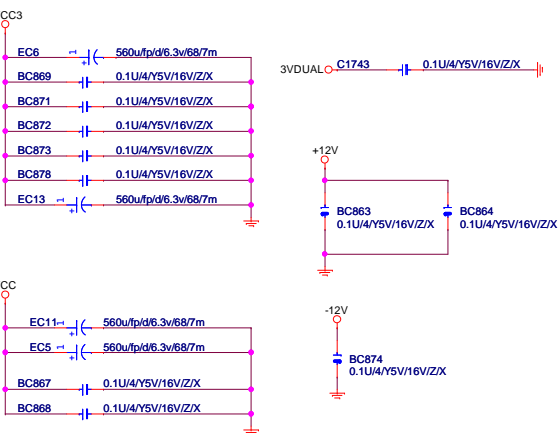
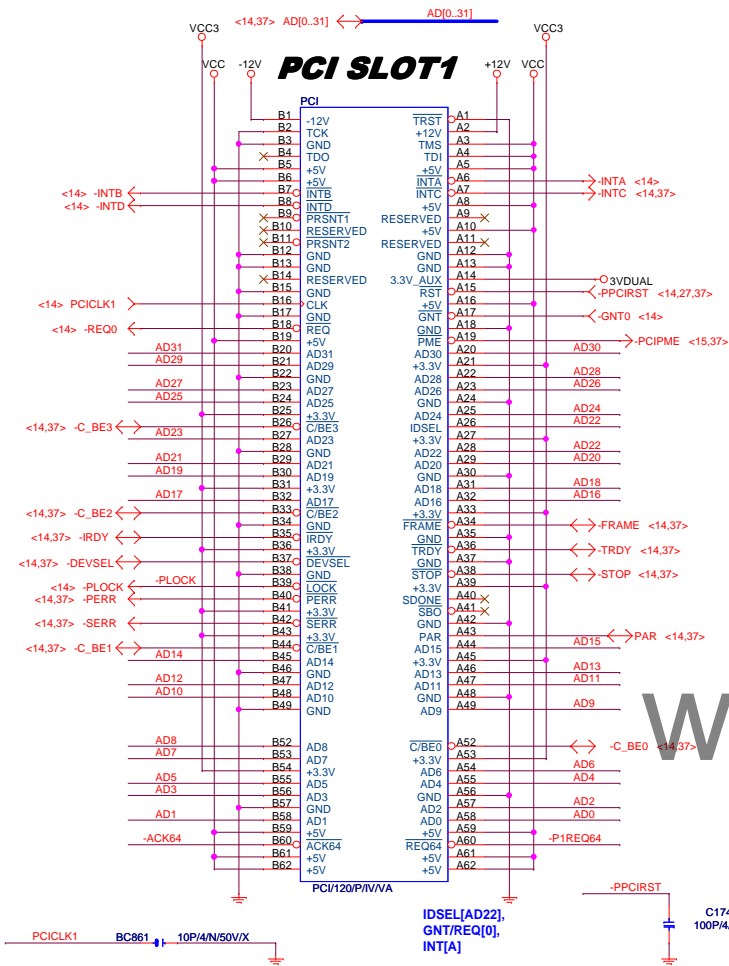
of

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PCI SLOT1



PCI SLOT 1,2

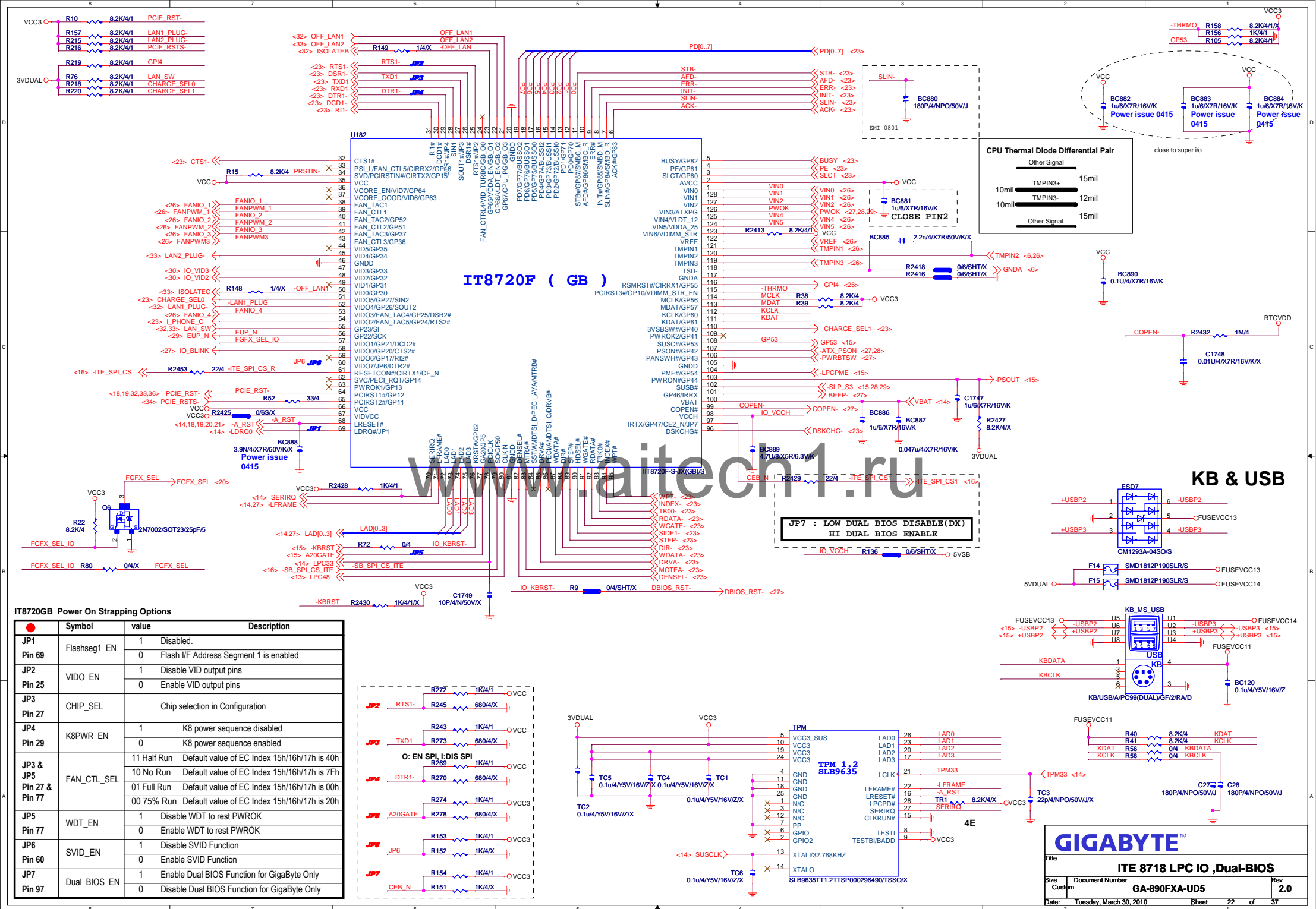
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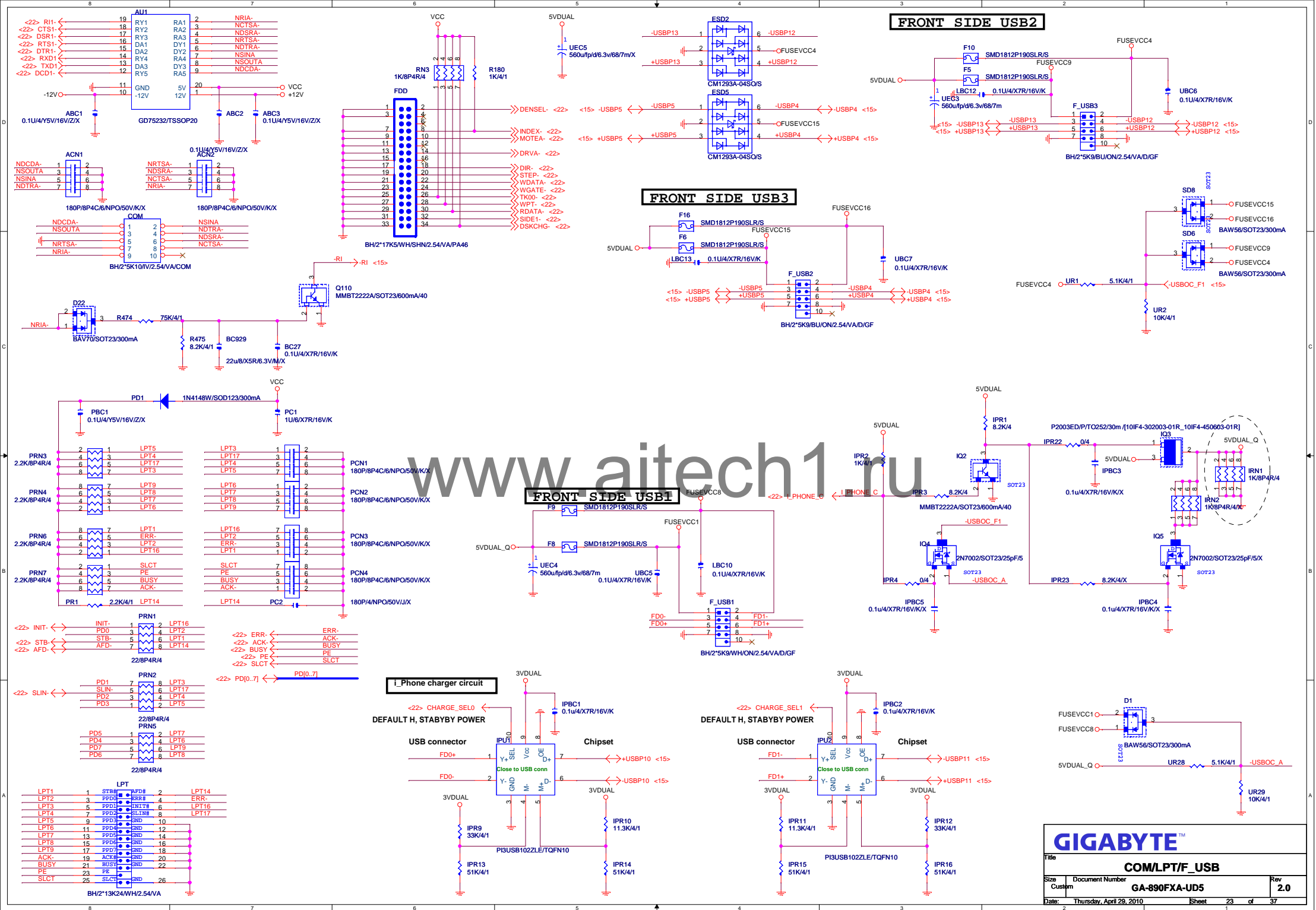
Document Number
GA-890FXA-UD5

Rev
2.0

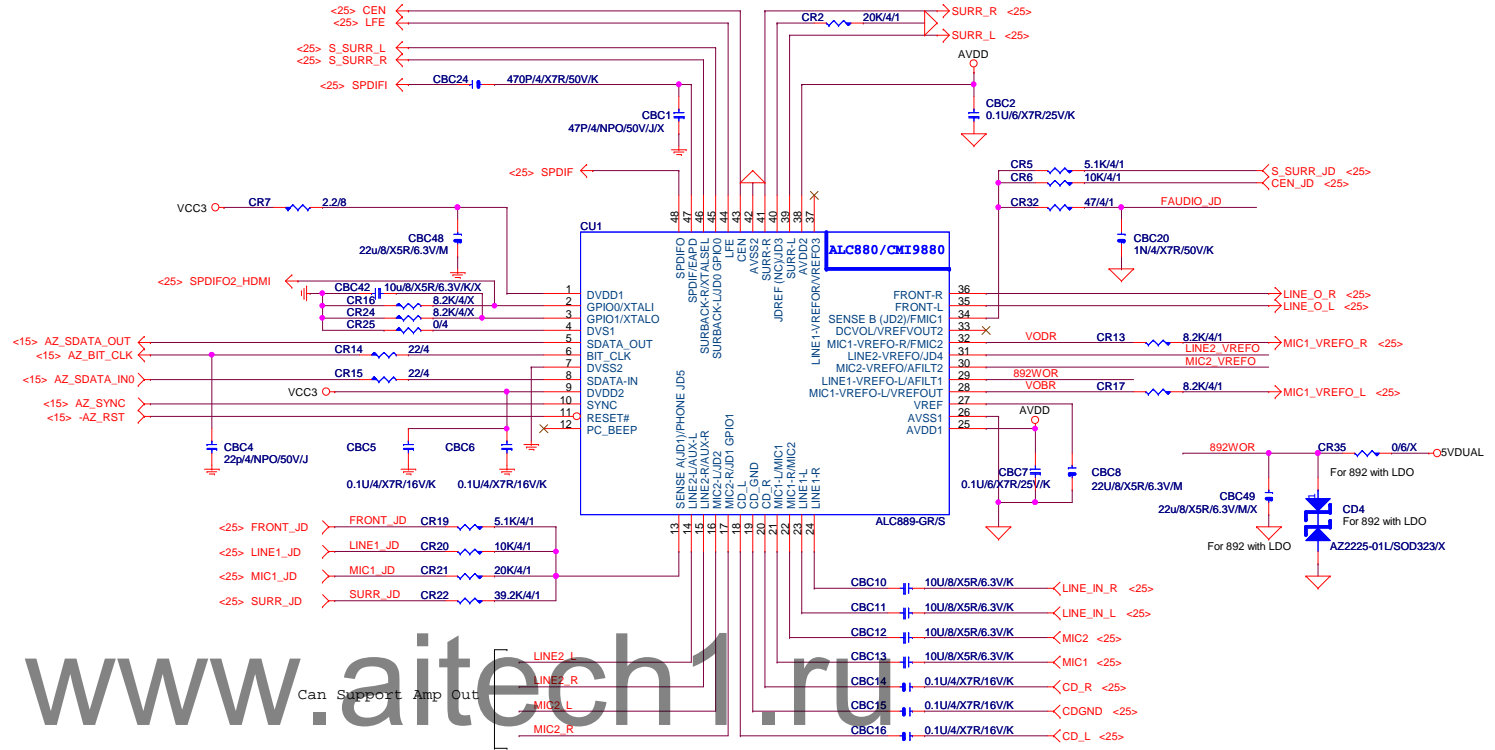
Date: Tuesday, March 30, 2010

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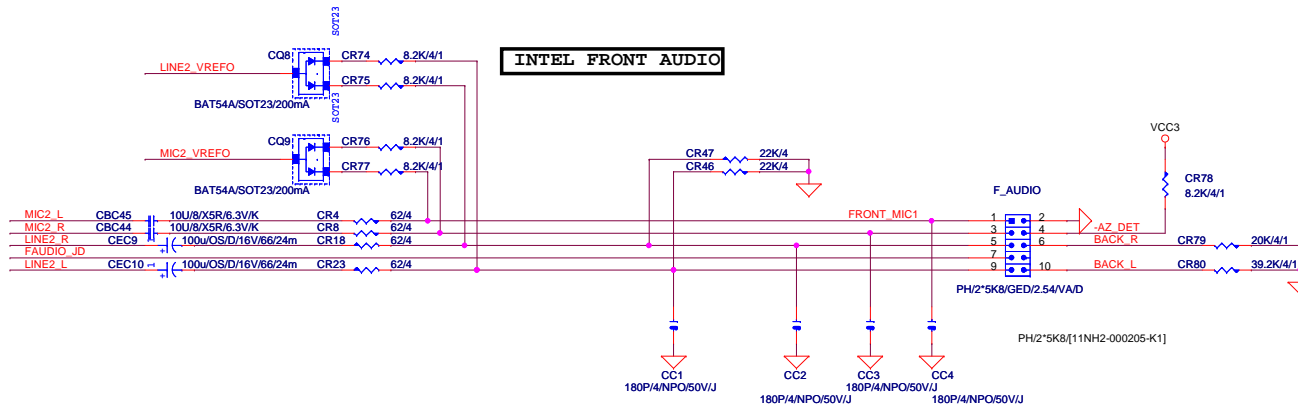


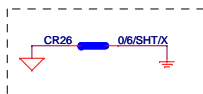


	ALC892	ALC889	ALC889A
CR16	X	X	O
CR24	X	X	O
CR25	X	O	O
CBC42	10uF/X5R	X	X
CR2	20K/1%	20K/1%	20K/0.1%
CR9	O	O	X
CR10	X	X	O
CBC10/CBC11/CBC12/ CBC13/CBC44/CBC45	4.7uF /X5R	10uF /X5R	4.7uF /X5R
CR4/CR8/CR18/CR23/ CR11/CR12/CR27/CR29/ CR49/CR50/CR43/CR44/ CR45/CR48/CR59/CR60	75 ohm	66 ohm or lower	75 ohm

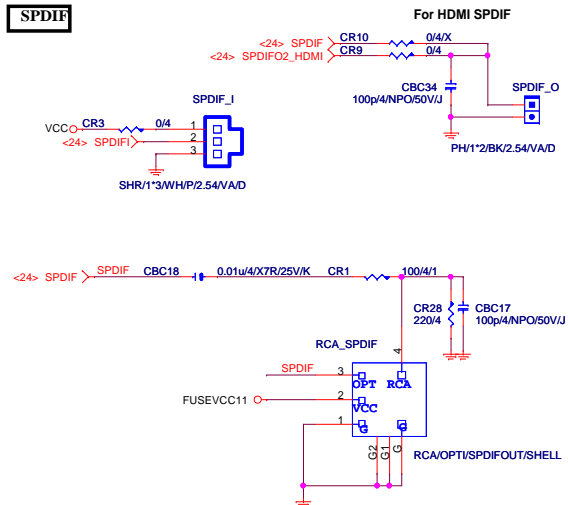


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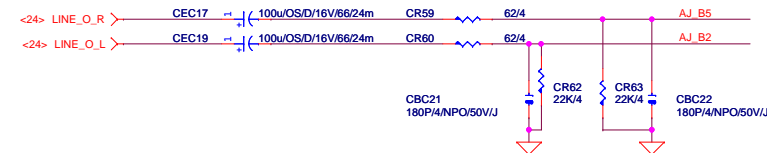




SPDIF



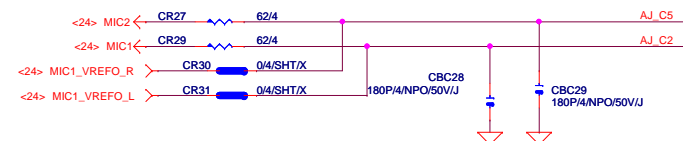
LINE OUT FRONT OUT



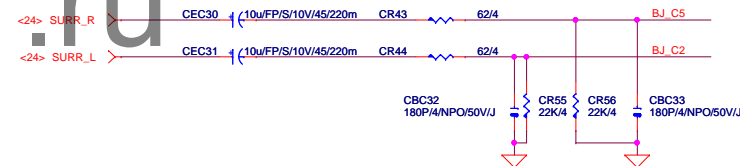
LINE-IN



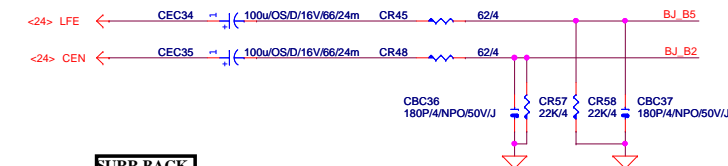
MIC



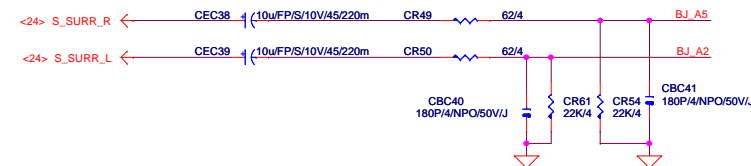
SURROUND



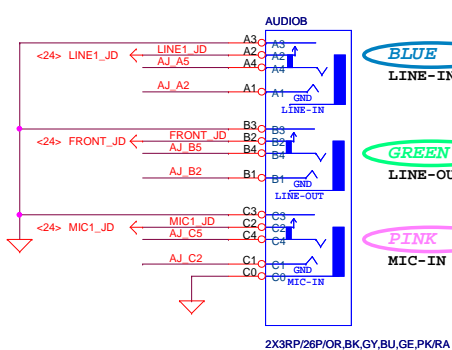
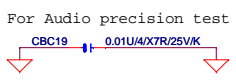
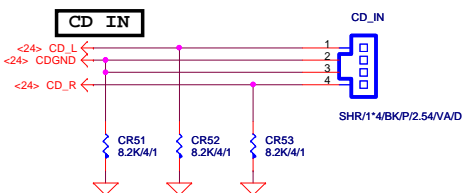
CEN/LFE



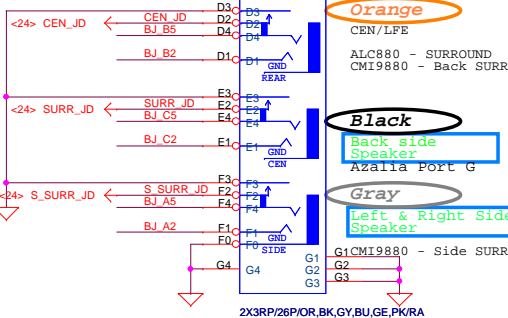
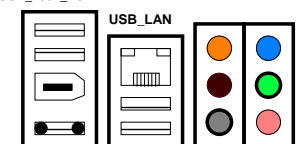
SURR BACK



CD IN



USB_1394_ESATA



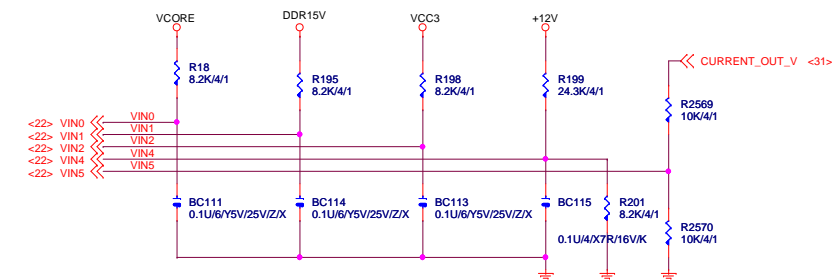
A3R7/13P/B/[11NR6-403006-01_11NR6-403006-02]
3R7+15P/[11NR6-403004-11]

A3R7/13P/0BG/[11NR6-403006-71]
3R7+15P/[11NR6-403004-31]

GIGABYTE

Title		
AUDIO JACK		
Size	Document Number	Rev
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Schematic diagram of the temperature sensor circuit for the B716 N/A. The circuit includes a VREF input, four temperature inputs (TMPIN1, TMPIN3, TMPIN2, and a combined TMPIN2/TMPIN3 input), and a common ground. The circuit components include resistors R203, R205, R206, RS1, SRS2, and R2253, capacitors C113, C114, C1080, and C1306, and two thermistors labeled SYSTEM Thermistor and CPU Thermistor. The R2253 resistor is highlighted with an oval and labeled '30K/4/X FOR B716 N/A'.

[illegible]

POWER FAN

+12V

R404
3.3K/4/1

+12V

R412
15K/4/1

R418
6.2K/4/1

C193
3.3N/4/X7R/50V/K

FAN1*3/WH/A3/PA66

FANIO_4 <<22>

PWR_FAN
FAN1*3/WH/A3/PA66

SYSTEM FAN2

+12V

R402
3.3K/4/1

+12V

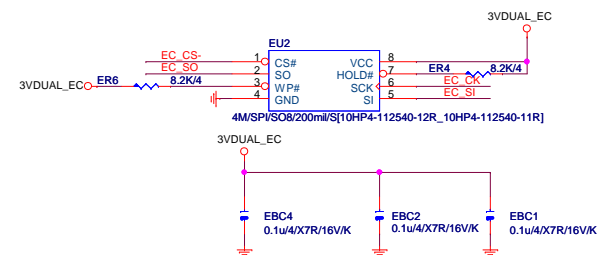
R410
15K/4/1

R415
6.2K/4/1

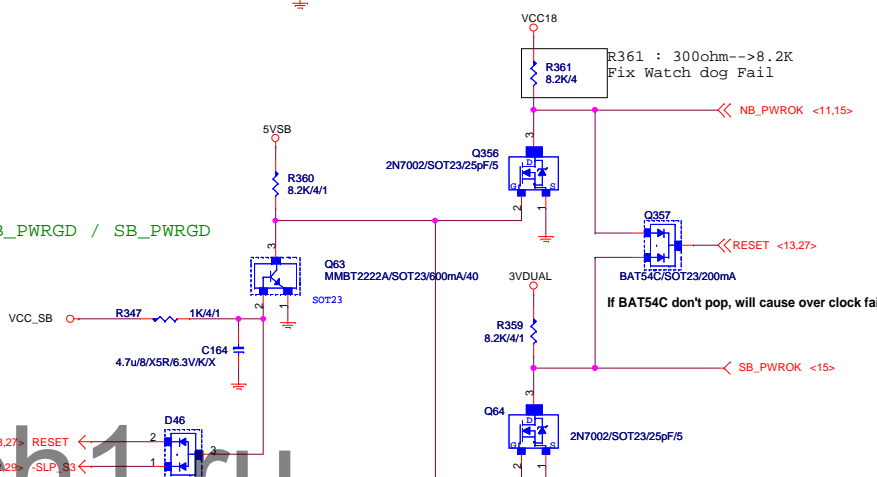
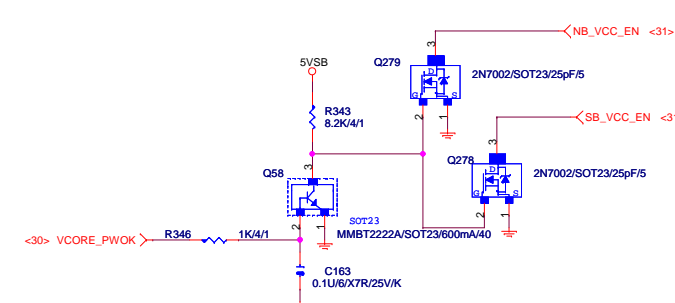
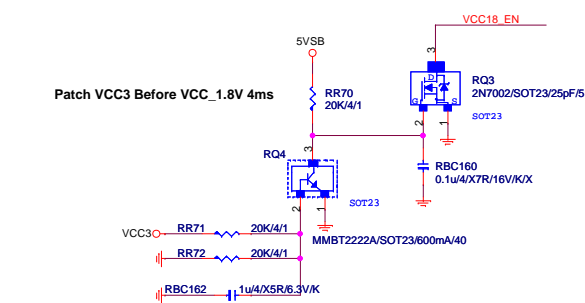
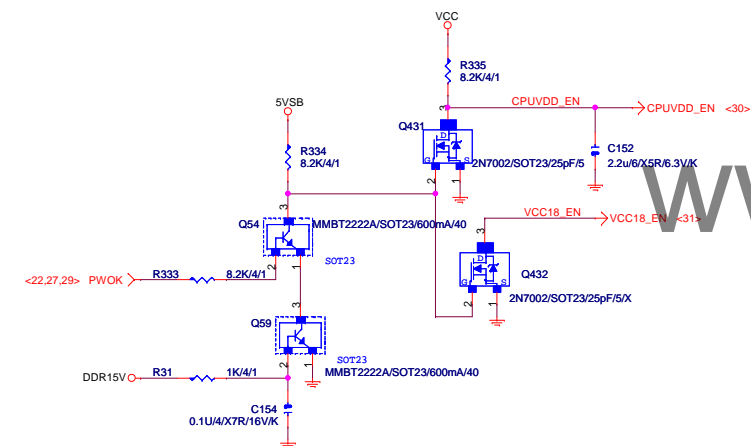
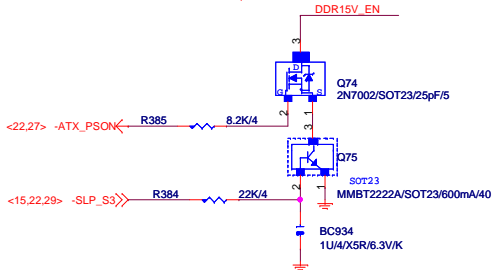
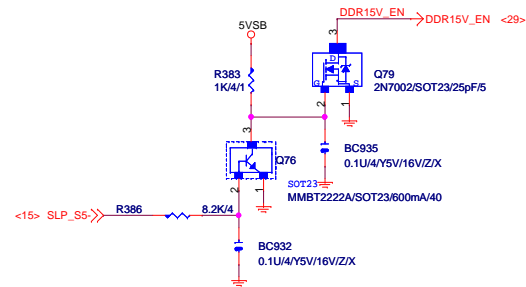
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C191
3.3N/4/XTR/50V/K

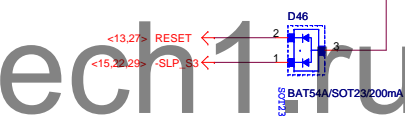
SYS_FAN2
FAN1*3WH/A3/PA66

[illegible][illegible]

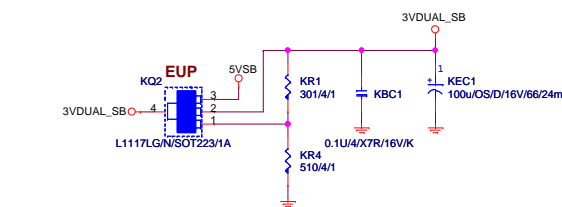
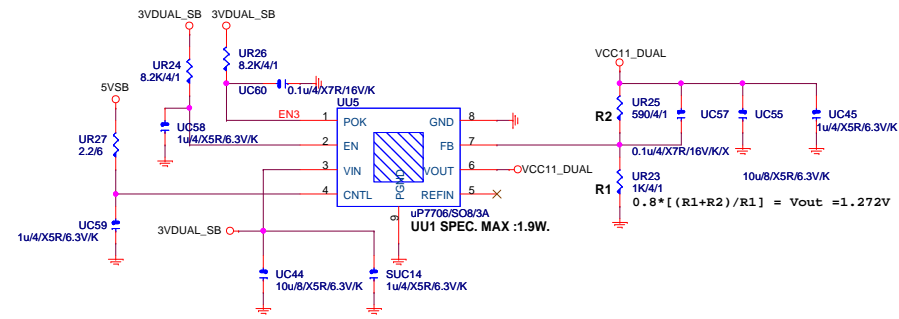
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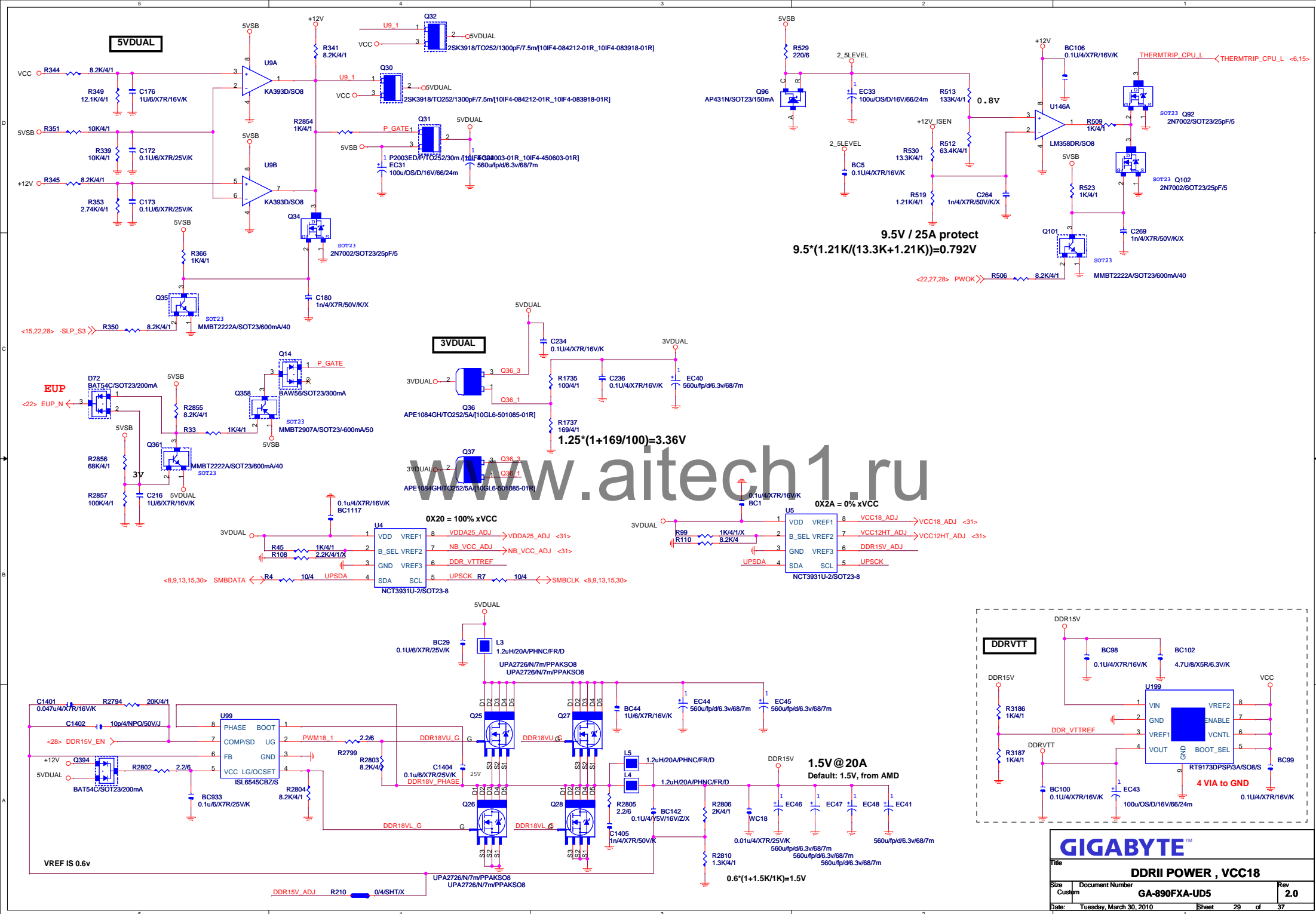


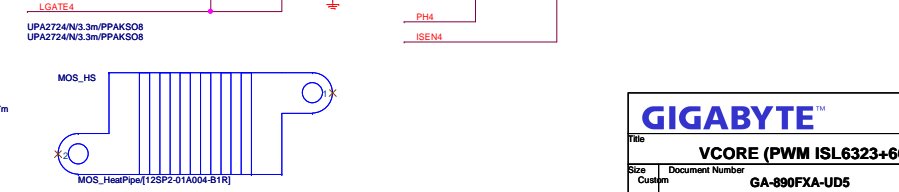
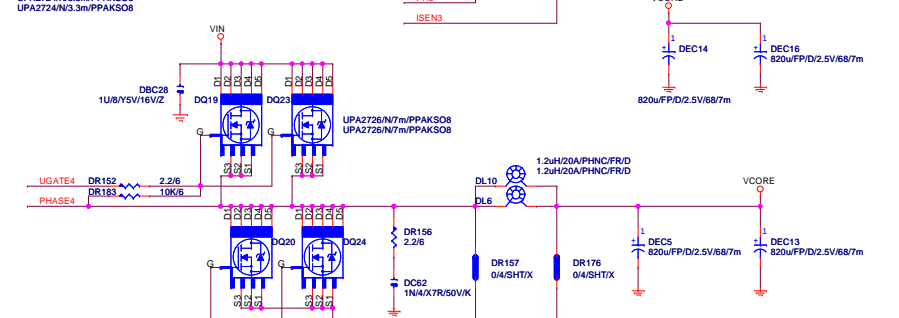
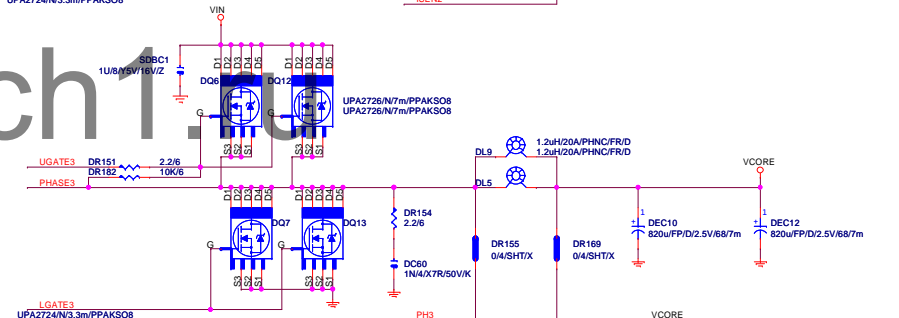
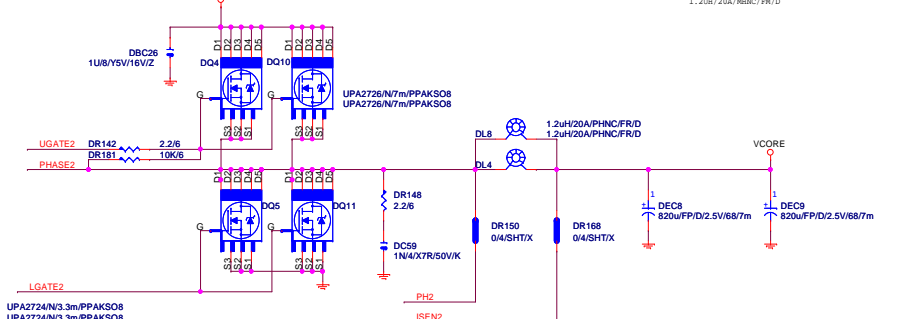
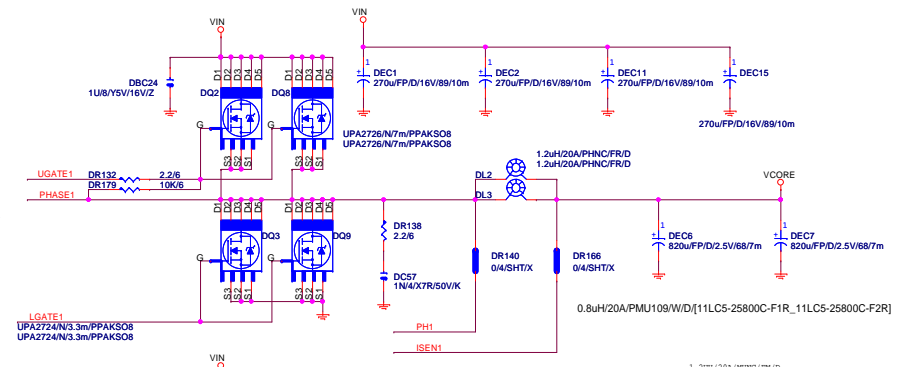
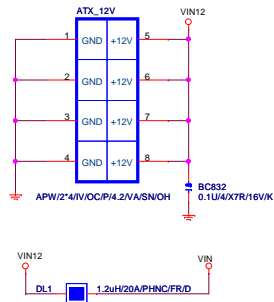
PWOK > NB_PWRGD / SB_PWRGD



(1.8V , 1.2V , 1.1V) > NB_PWRGD 前 1ms





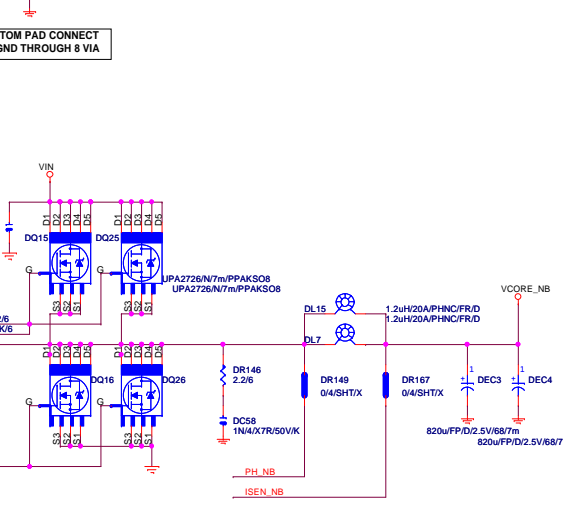
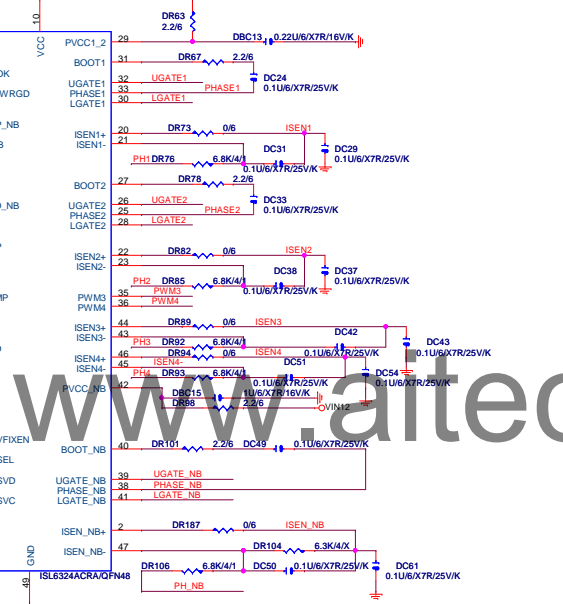
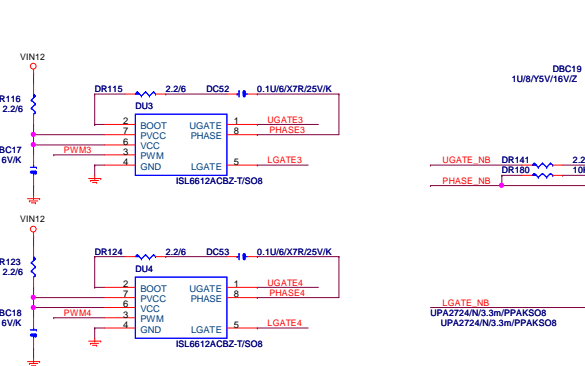
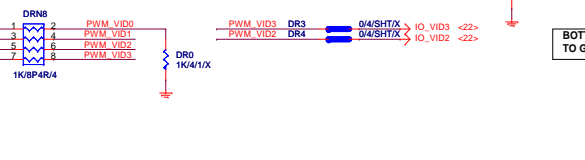
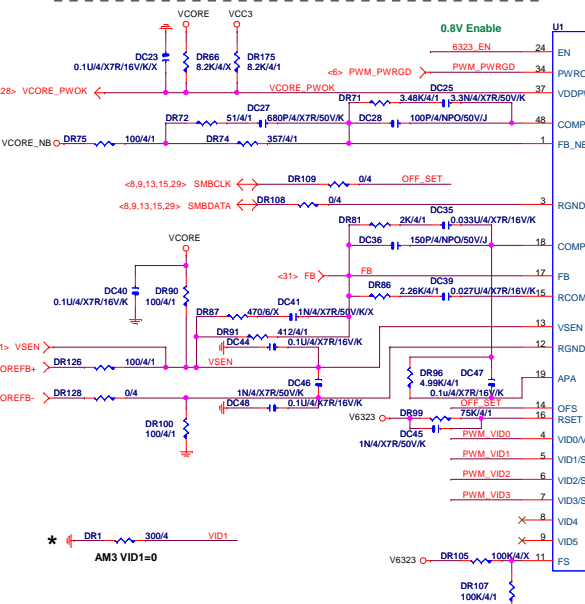


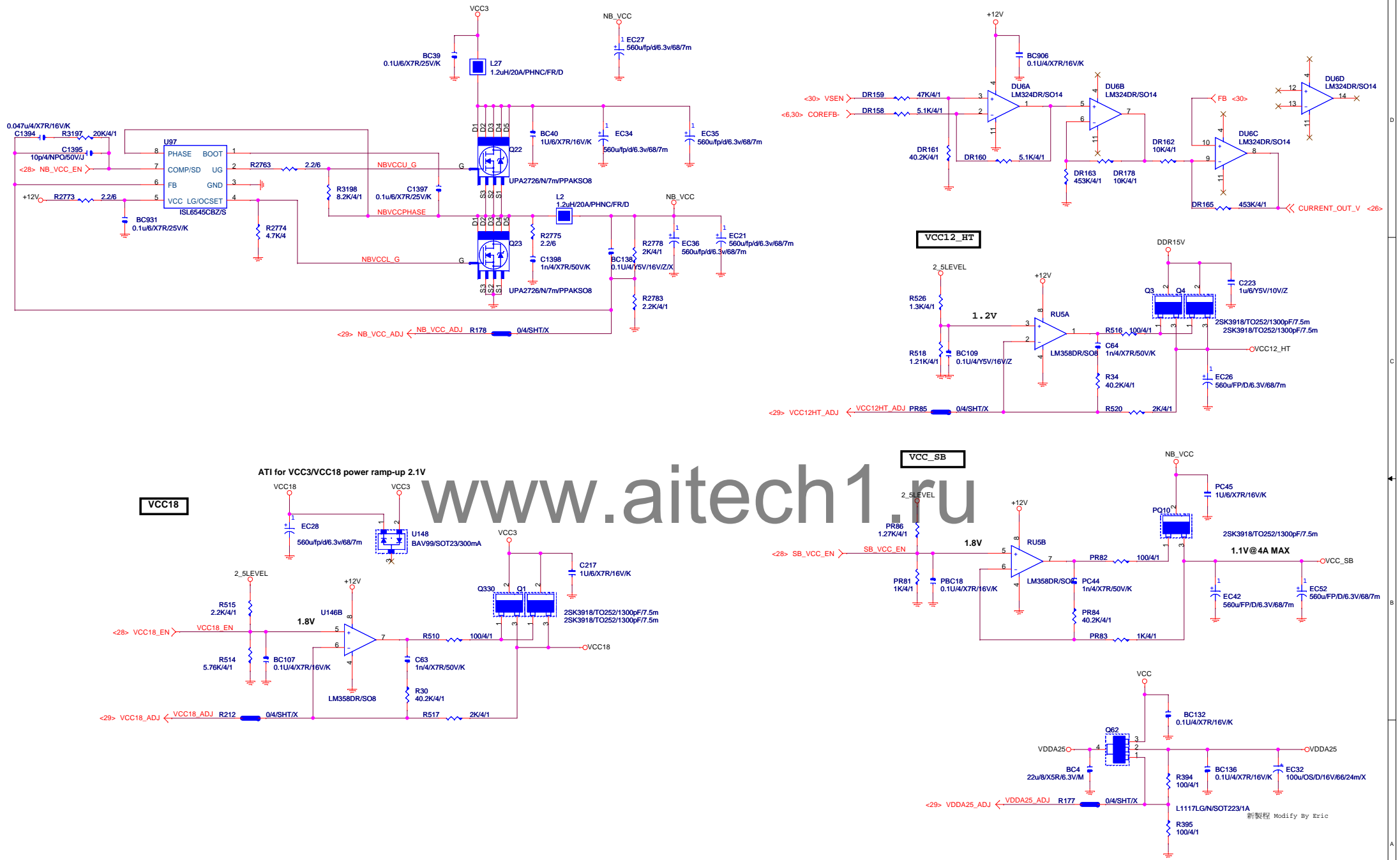
28 CPUVDD_EN CPUVDD_EN DR2 0/4 6323_EN

PWROK (SVI)
Low: "metal VID"
High: running protocol

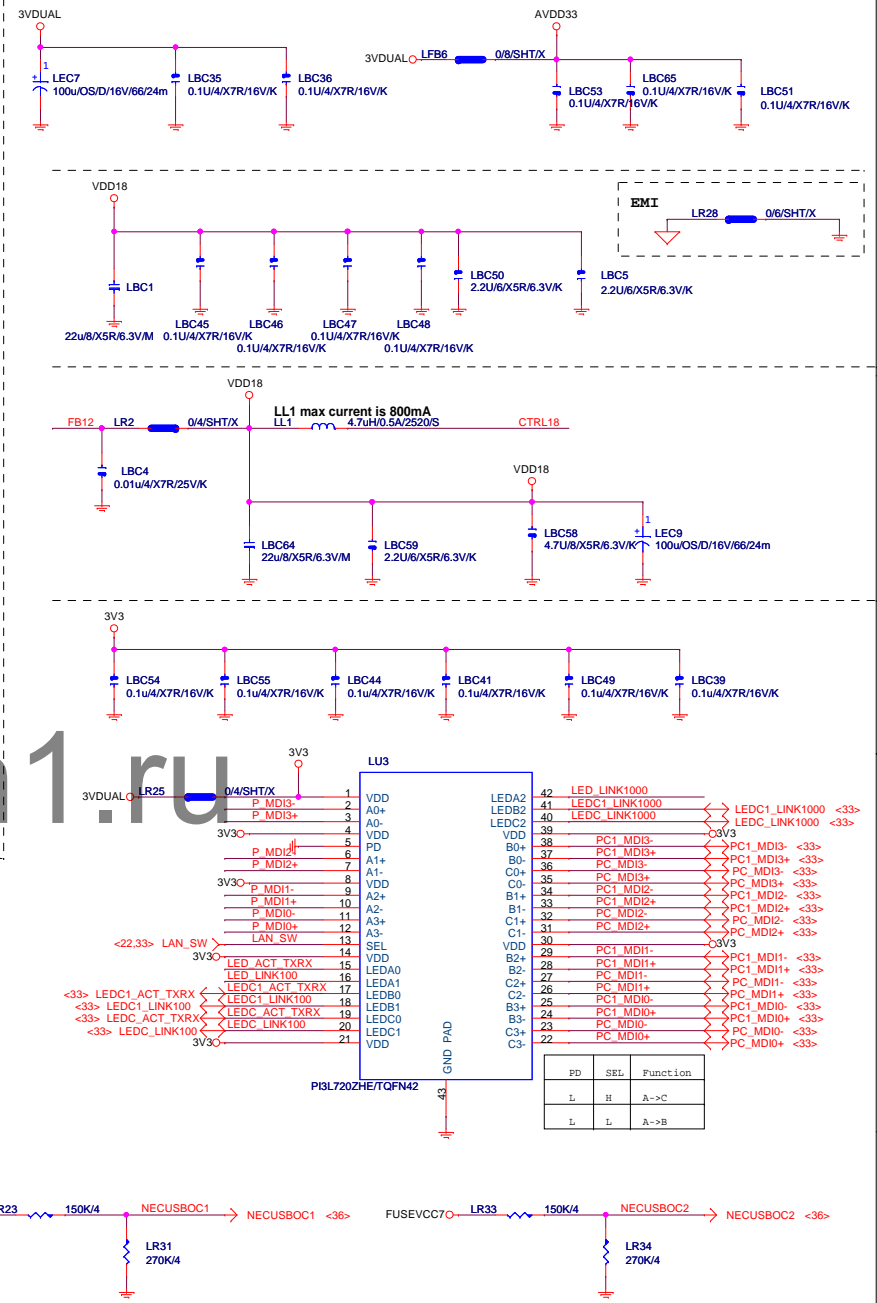
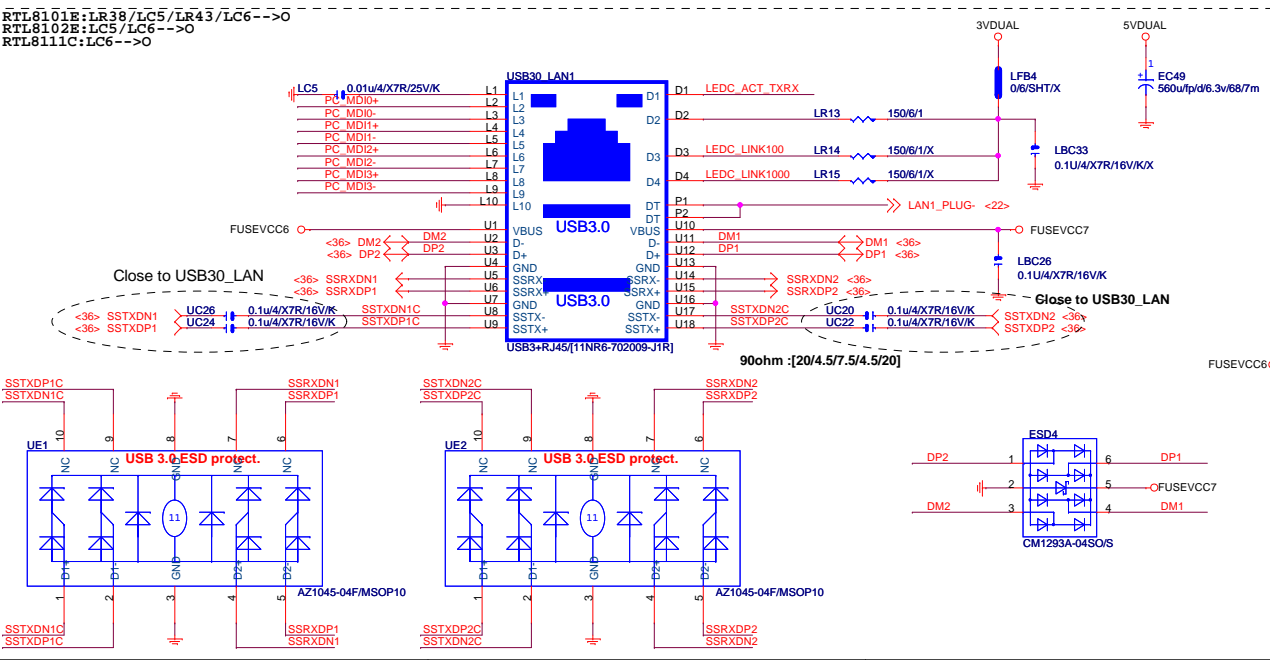
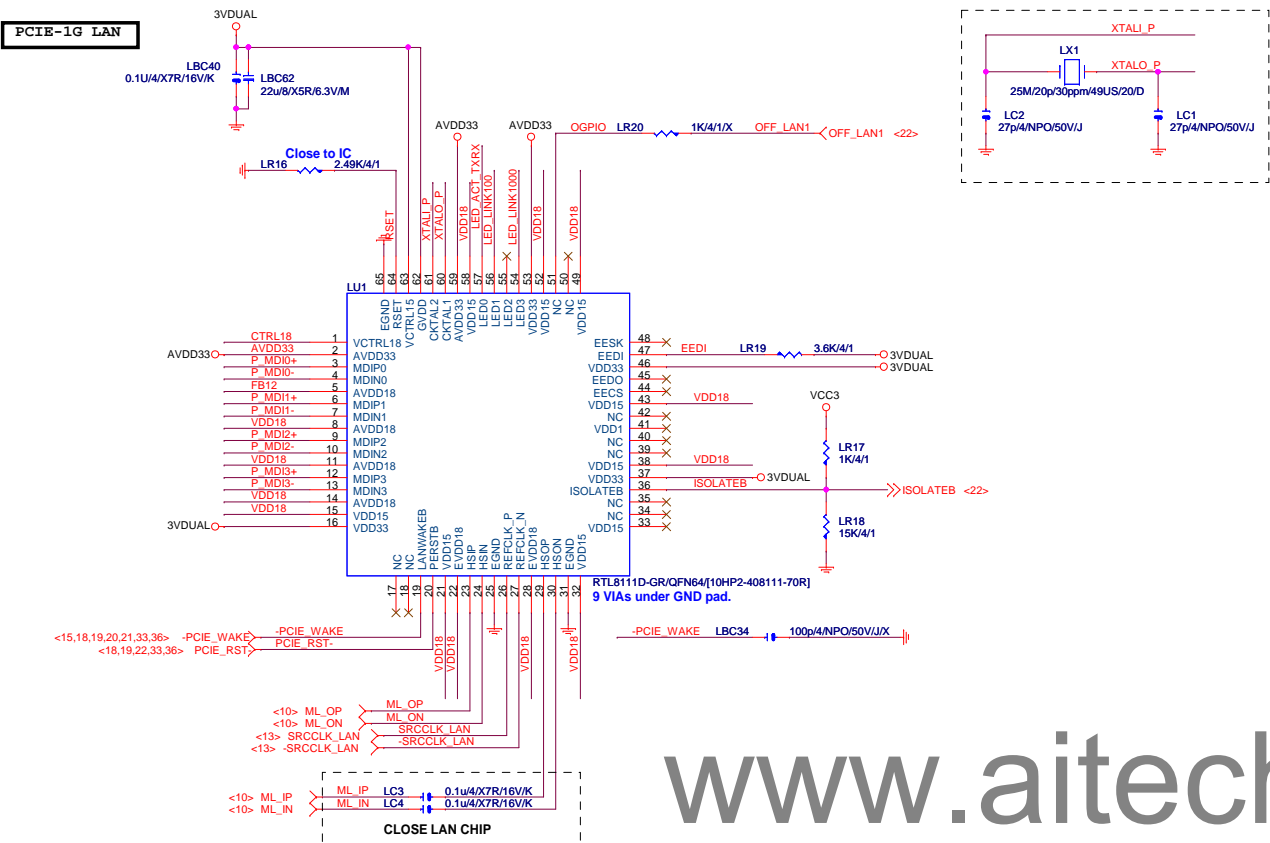
EN rising edge:
HI: PVI mode
Low: SVI mode

Pin 34 Input, Pin 37 Output





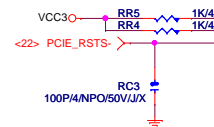
PCIE-1G LAN



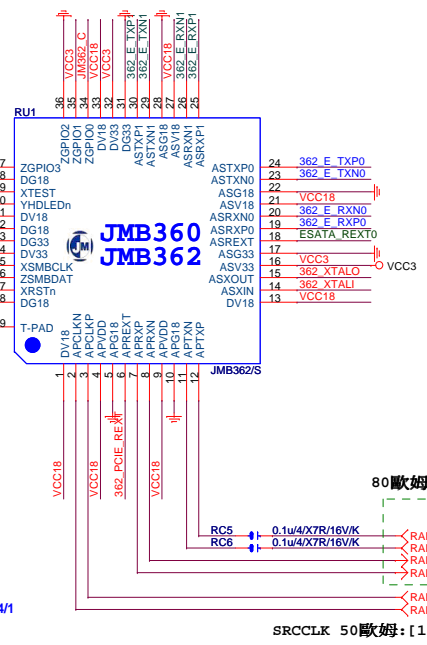
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SMBUS for test mode only.



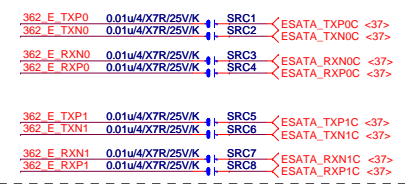
Near to PIN
Check SATA eye
PCIE_REXT -> 8.06K/4/1



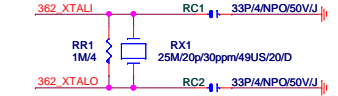
SRCCLK 50歐姆: [18/4/10/4/18]

Close to connector

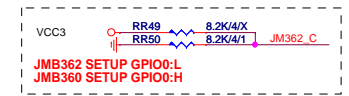
100ohm: [15/4/10/4/15]



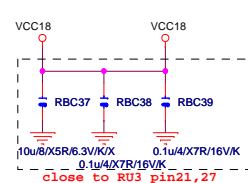
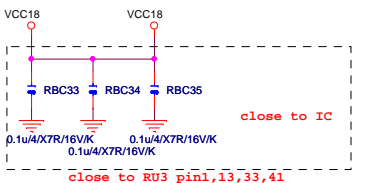
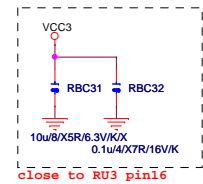
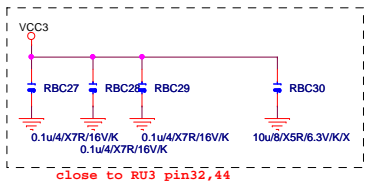
Close to JMB360/2 pins (<500mil)



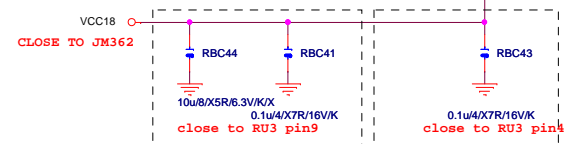
VCC3 -> RS51 8.2K/4/1 JSATA_LED



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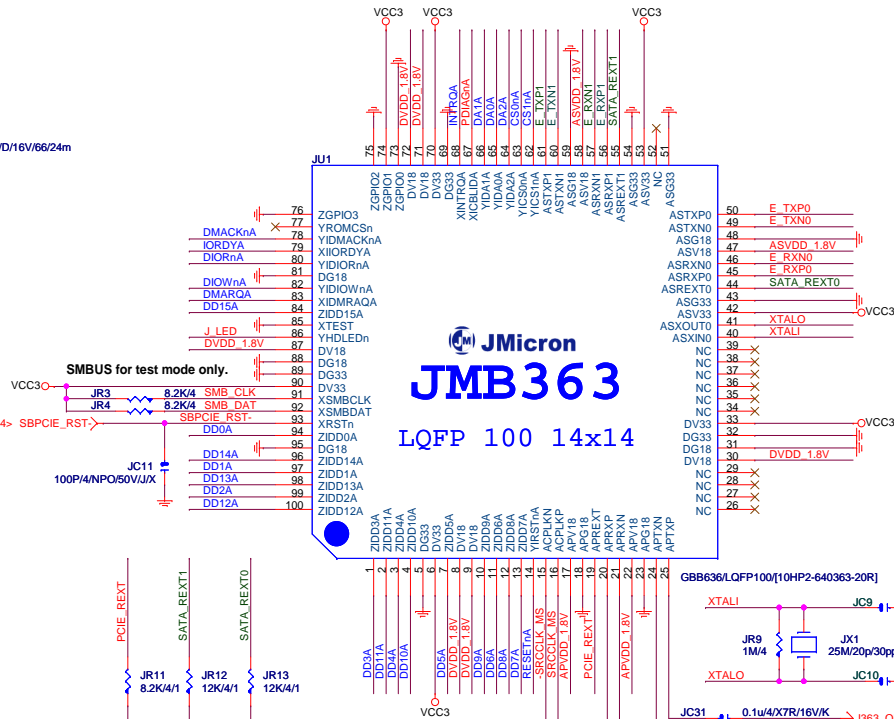
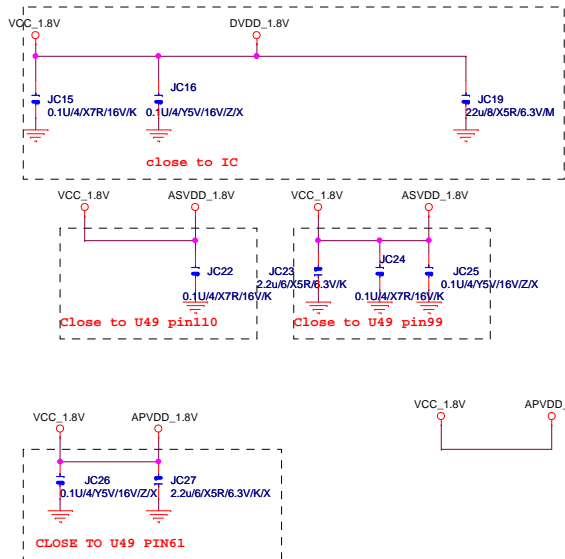
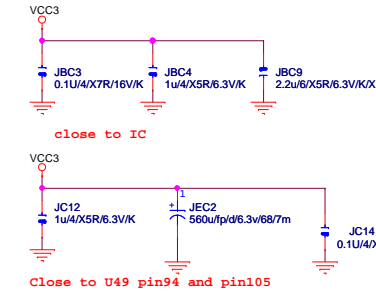
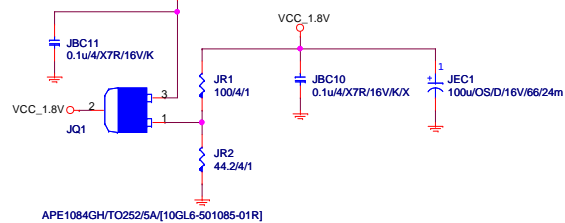


362_ASVD_1.8V
362_DVDD_1.8V

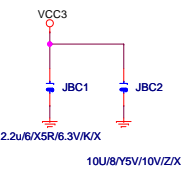


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3.3V to 1.8V Voltage Regulator



Near to PIN Check SATA eye
PCIE_REXT → 8.06K/4/1



JMicron
JMB363
LQFP 100 14x14

